

http://www.users.on.net/~glenk/millerloop/millerloopstability.htm

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APR JUL AUG

11

2013 2015 2016



About this capture

7 captures

19 Sep 2012 - 11 Jul 2015

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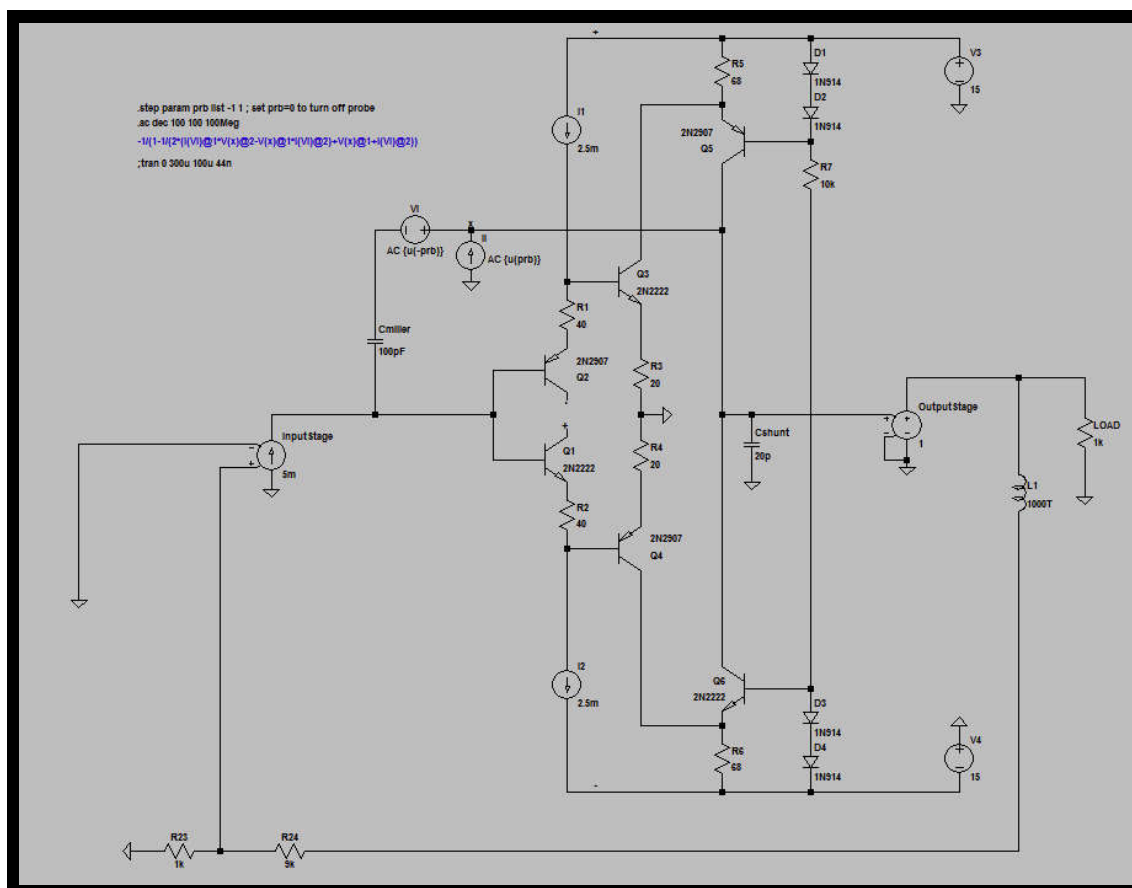
—Brewster Kahle, Founder, Internet Archive

Transimpedance Stages

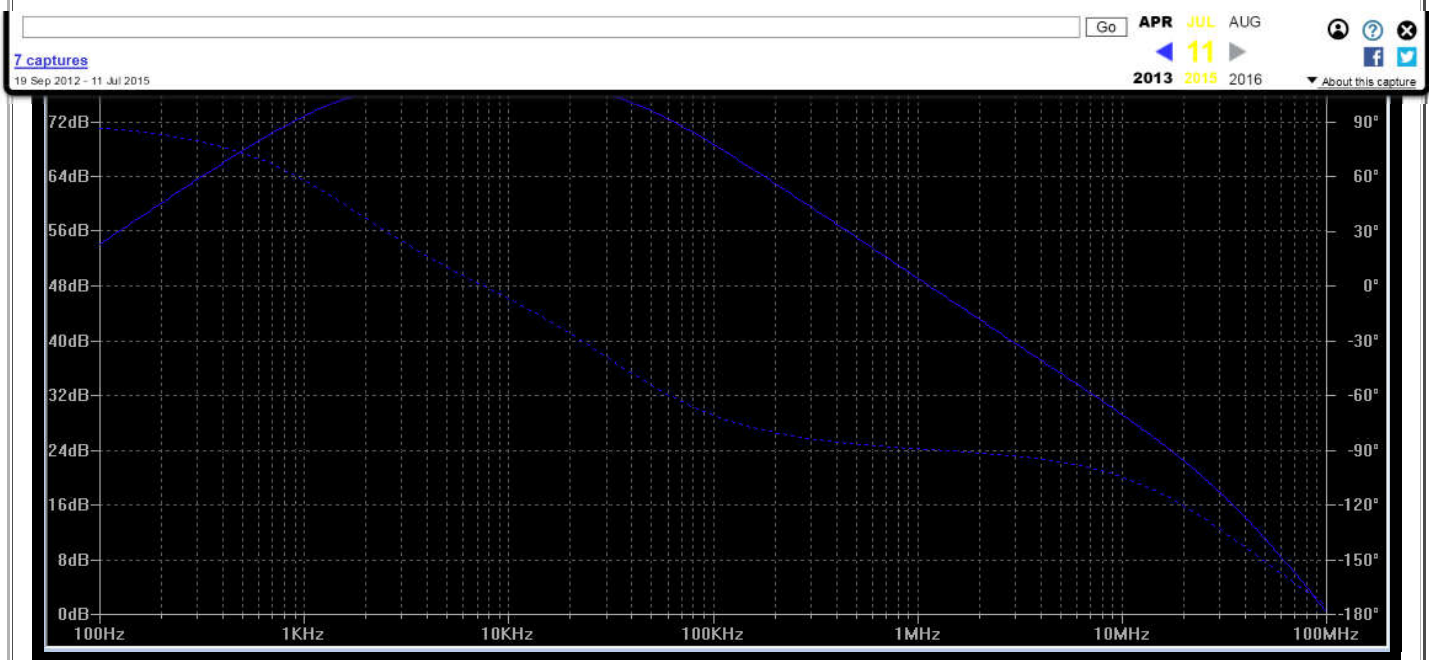
u.net

closed loop gain of 20dB and a unity loop gain frequency of dductance.

is disabled for AC by L1 and the loop gain probe is placed in



Here is the result:

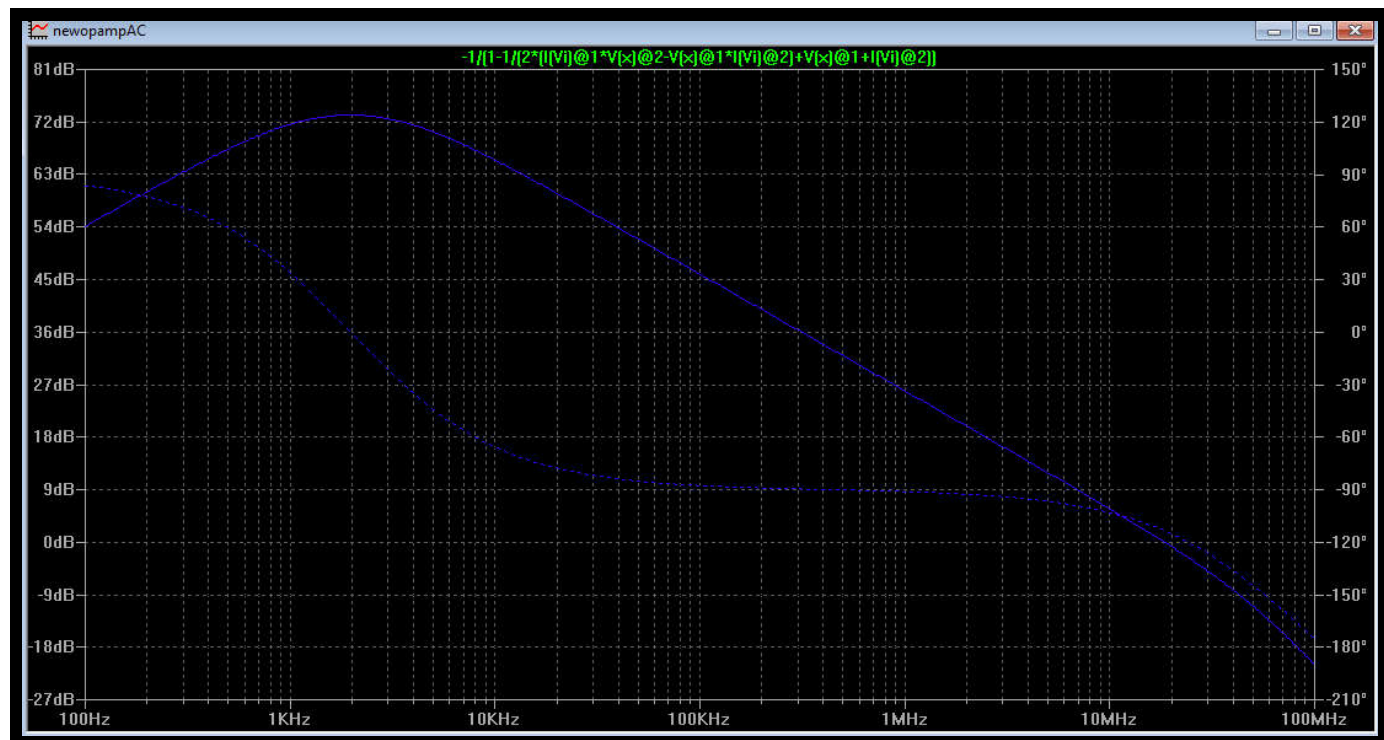


Observations:

The Miller compensation loop is not stable - the unity loop gain frequency is 100 MHz (Eeeek!) and the phase margin is about zero.

Solutions?

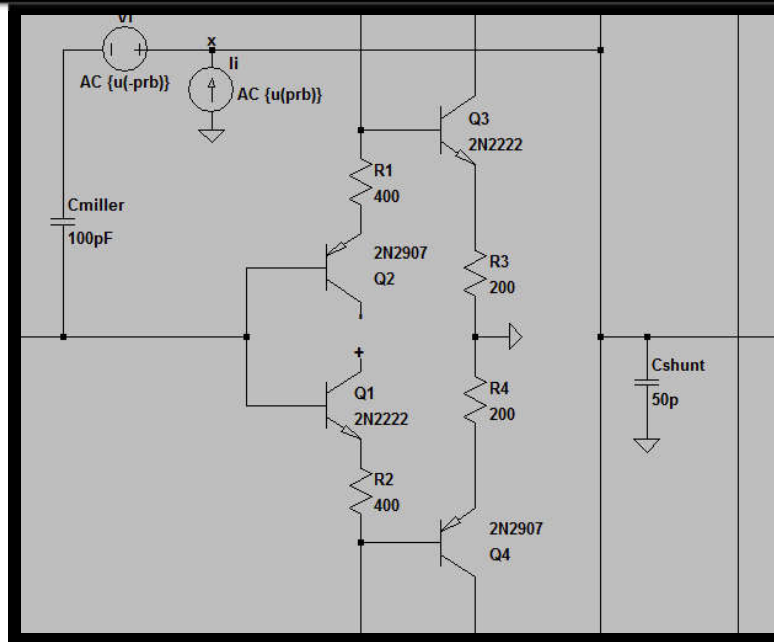
#1 - increase the TIS load capacitance (Cshunt) from 20 pF to 500 pF to kill the HF loop gain of the TIS. Note that Cshunt does not add another "pole" to the response - as far as the output node of the TIS is concerned, it is just an additional amount of capacitance effectively in parallel with Cmillier.



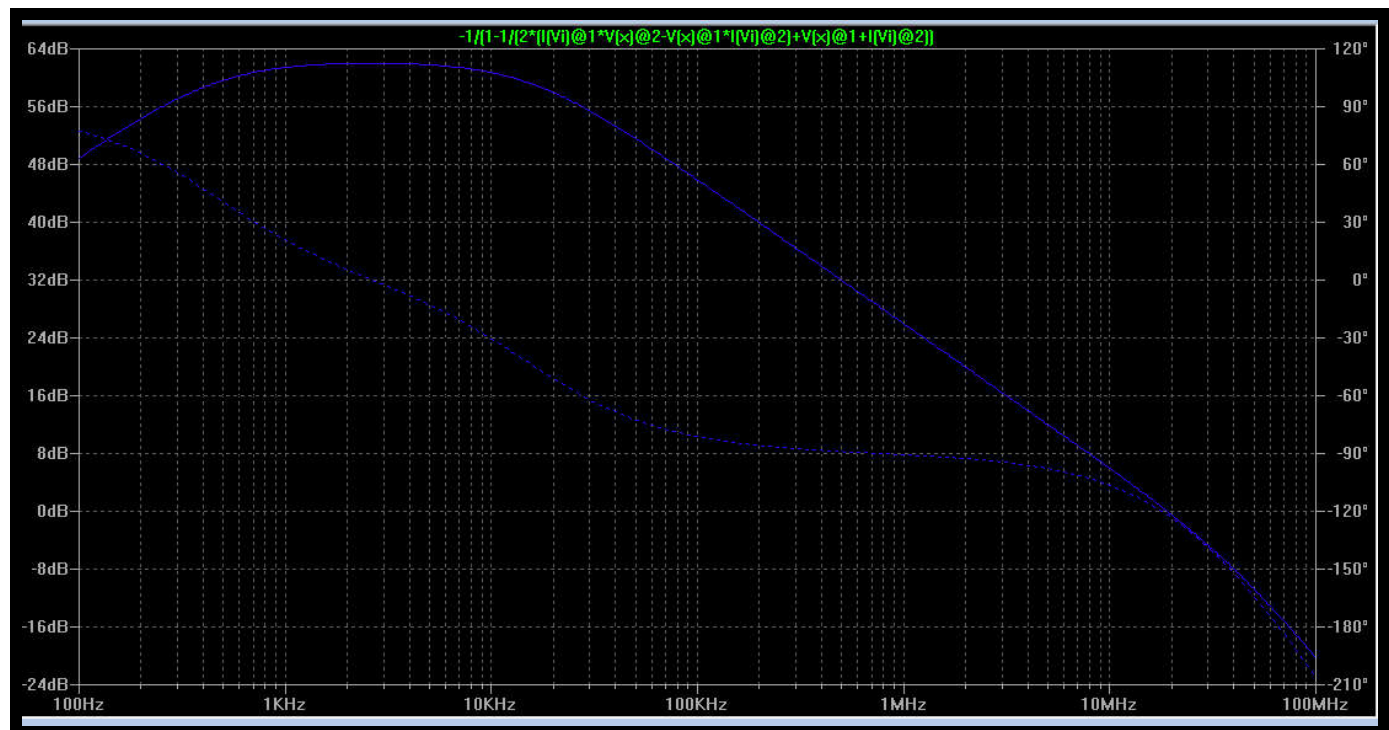
Now that looks a bit better! The unity loop gain frequency has been reduced to a bit under 20 MHz and the phase margin is better than 60 degrees. The TIS is comfortably stable.

The TIS is now stable, but with what compromise? 500 pF is a lot of capacitance to plonk at the output node of the TIS and will cause a lot of unnecessary distortion at high frequencies due to the additional loading. A very important observation however: TIS stability can depend very much on there being a large shunt compensation capacitance present at the output node. In a power amplifier, this shunt capacitance can be provided by the input capacitance(s) of the driver transistors of the power output stage; A possible advantage of a "Double EF" output stage over a "Triple EF" output stage - keep in mind that a TIS driving the latter may need to be augmented with Cshunt for Miller compensation loop stability reasons.

Q:But is there a better way to make the TIS stable?



The result:



As theory predicts, we have the same level of stability in the Miller compensation loop with ten times less Cshunt. Yahoo.

But is there a trade off? Yes - the output impedance of the TIS will not be as low throughout the audio frequency range due to both the increased emitter degeneration of the common-emitter voltage gain stage(s) and the reduced loop gain. However this is the price one pays for a healthy phase margin and stability. It's worth noting that the simulation as present thus far is a simplified one that does not take into account aspects of PCB layout. However, in practice, I have found it to be an entirely reliable predictor of performance and stability, for practical PCB layouts using either SMD or through hole components so long as the unity loop gain frequency of the Miller compensation loop is conservatively designed to be in the region of 10 to 20 MHz, which quite suffices for any audio application.

That's all for now..... to be continued.

Go

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