

Audio amplifier topology with push-pull transimpedance stage – Part 3: Experimental verification

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9. Experimental Verification

To compare the audio performance of the new transimpedance stage to the standard amplifier topology from figure 1, a model amplifier (that is, an amplifier with a small-signal output buffer only, which is powered from low voltage regulated supplies [1]) for each topology was built. Figure 11 depicts the implementation which was chosen for the standard topology, and in figure 12 the model amplifier for the novel transimpedance is shown.

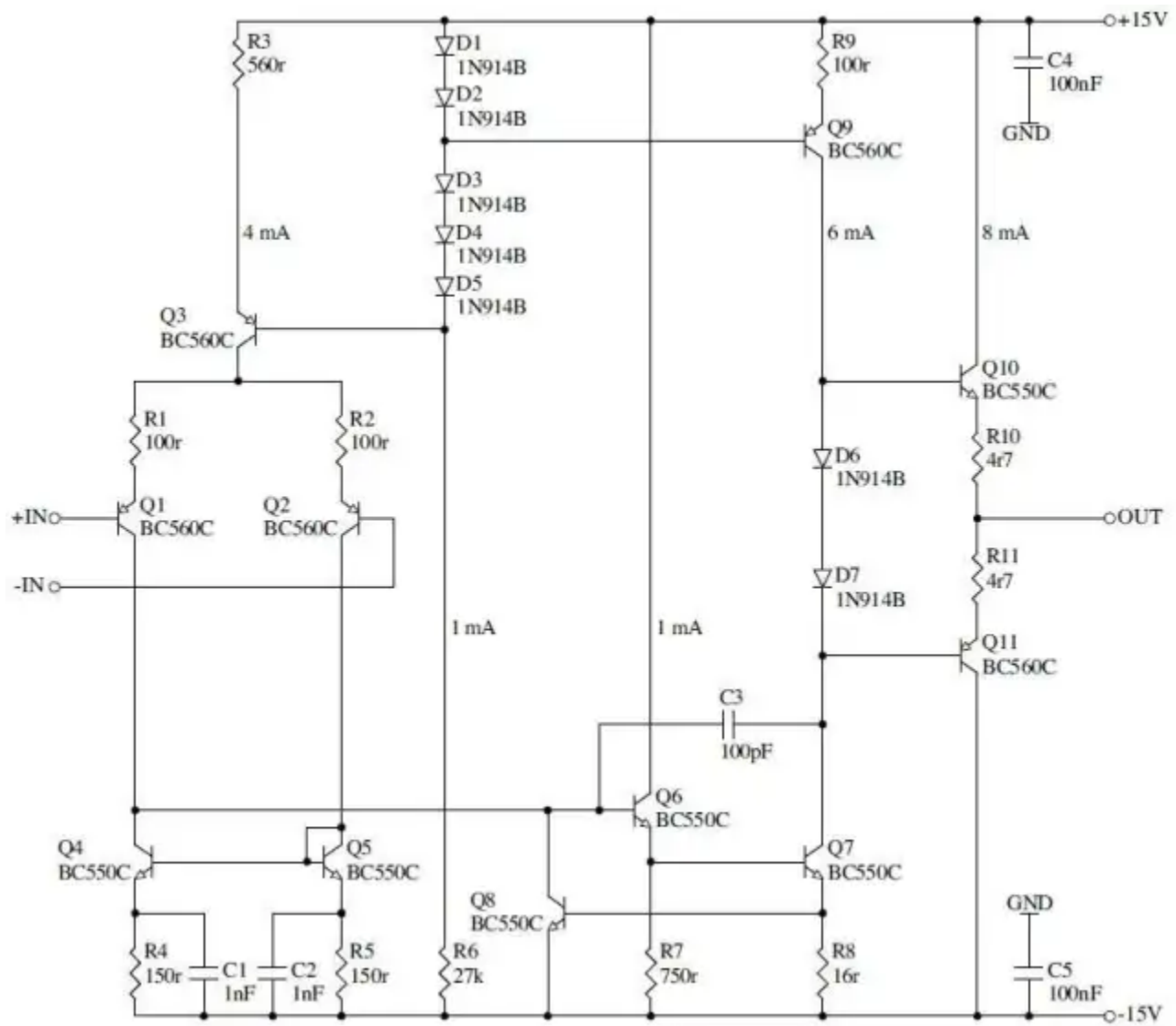


Figure 11: Model amplifier implementation for the standard two-stage topology.

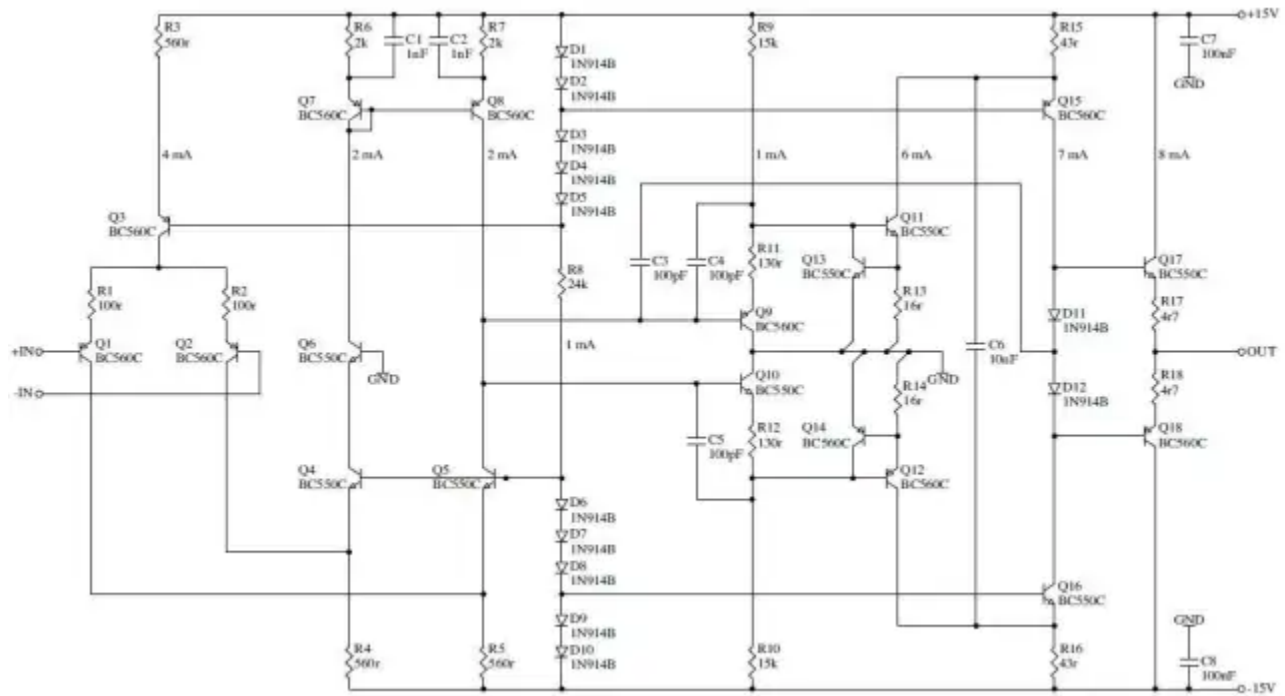


Figure 12: Implementation of the model amplifier for verification of the new transimpedance stage.

To make the results as fair as possible, the input differential pairs have the same quiescent current and emitter degeneration, and the compensation capacitors have alike values. Furthermore, the quiescent current of the emitter followers and the common emitter transistors in the transimpedance stage, as well as the emitter resistor values of the common-emitter transistors, are made equal. Obviously, also the small-signal class A output stage details are equivalent. For simplicity, the use of voltage regulators for the front-end of the new amplifier was omitted. If measured at a noise gain of 22 (which gives a unity loop gain frequency of about 700 kHz), +20 dBu output level and within a 80 kHz bandwidth, THD+N of both amplifiers is below -112 dB across the full audio frequency range, and dominated by amplifier noise and residual contributions of the oscillator and analyzer. This indicates that both topologies have no inherent distortion mechanisms in the small-signal stages which were significant in the context of a full power amplifier design. Substantial differences however are observed if the two amplifiers are evaluated for their sensitivity to loading at the second stage output node. In [5] I have introduced the use of a voltage-dependent network, consisting of two back-to-back connected 3.3 V zener diodes in series with a 10 kΩ resistor, to roughly model the loading behaviour of power output stages. There is no reason to suspect that this modeling is particularly accurate, however it enables the easy comparison of amplifier topologies regarding the sensitivity to this distortion mechanism, which is just what we need here. Figure 13 discloses the measurement results; without doubt they provide little evidence for arguing against the novel transimpedance stage.

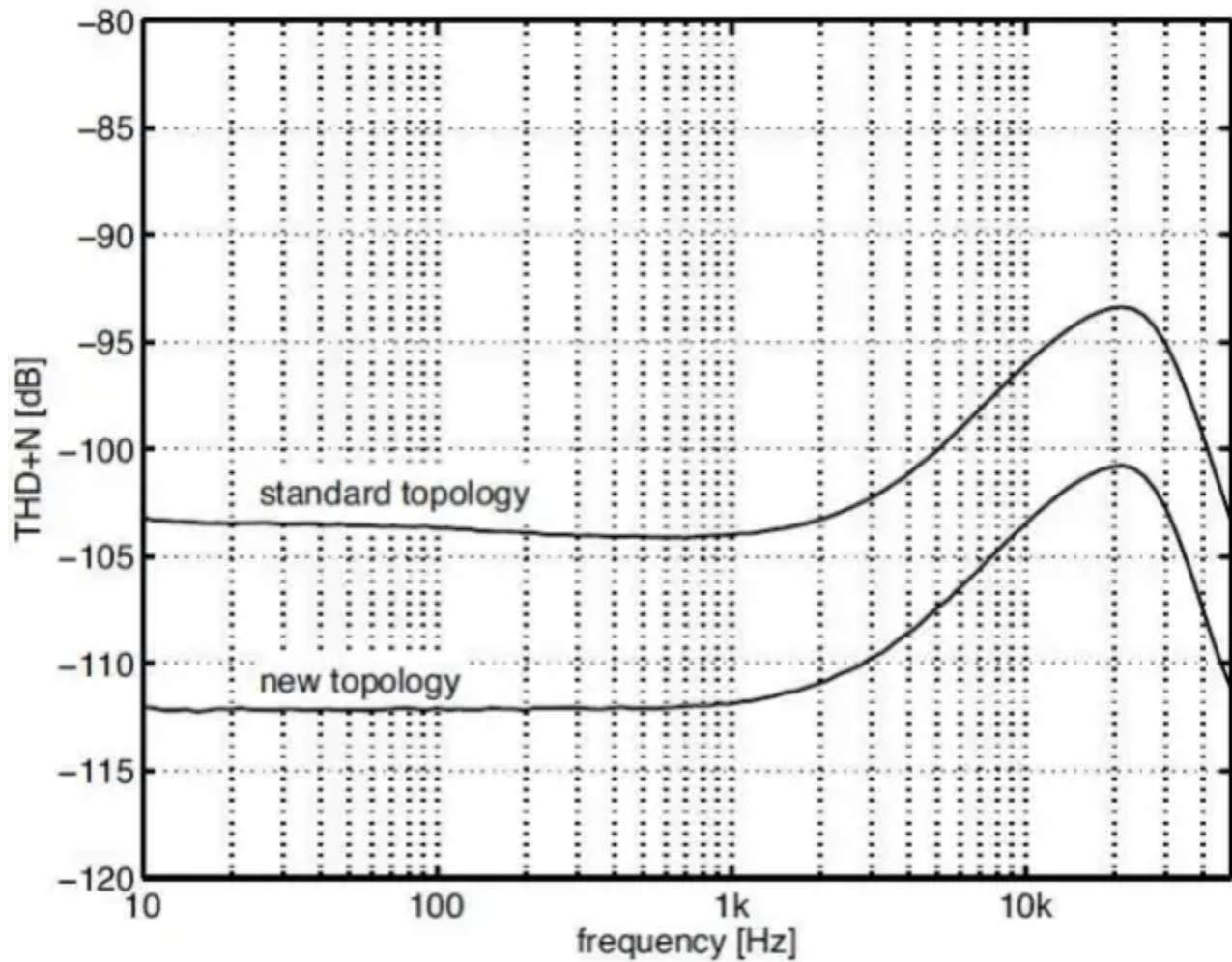


Figure 13: THD+N measurement (+20 dBu output level, 80 kHz measurement bandwidth) of the two model amplifiers with voltage-dependent loading of the second stage output node.

At low frequencies, the standard amplifier topology shows a mixed distortion residual, while the new amplifier architecture is still limited by noise and oscillator/analyzer contributions. Above 1 kHz, both model amplifiers show increasing distortion levels, however the magnitude observed for the novel transimpedance stage remains about dB below that of the conventional arrangement. Note that the decrease in distortion above 2 kHz is due to the bandwidth limiting filter and not actual circuit behaviour.

Unfortunately detailed discussion of the reasons which lead to the superiority of the new second stage with regard to output loading are beyond the scope of this article. I can just refer to the analysis I presented in [5], and give some food for thought in the following listing:

- The lumped resistance at the input node of the second stage is considerably higher for the new topology; this is because of the use of folded cascodes (which have higher output resistance than a differential pair), the current mirror with high emitter resistor values (which increases its output resistance), and the high-value resistors which are used to bias the emitter followers (R9 and R10 in figure 12). The high lumped resistance leads to low second stage output impedance.
- The complementary push-pull arrangement further reduces second stage output impedance, and mitigates the dependence of output impedance on output current.

- The novel transimpedance stage shows reduced nonlinear modulation of the compensation capacitor reference voltage (i.e. the second stage input node voltage). This is because the complementary topology cancels even-order harmonics present at the transimpedance stage input node.

Next I have evaluated the equivalent input noise of both amplifiers. Measured in a 22 Hz to 22 kHz bandwidth, the amplifier from figure 11 achieves -122.6 dBu (this includes the noise from the feedback network, with an effective total resistance of 98Ω). While this is already an excellent figure, the new amplifier topology does even better with -124.5 dBu.

This surprisingly large difference cannot be attributed to the input differential pair, as its implementation is equal for both amplifiers, and spread in transistor performance is probably lower than the measured deviation. To the extent that I have investigated this, I can explain the observed behaviour with the current mirror noise contribution. As noted in section 4, the new amplifier topology allows the choice of much larger emitter resistors for the current mirror (for the presented implementations the values are $2\text{ k}\Omega$ for the new push-pull stage, and $150\ \Omega$ for the standard amplifier), which reduces current mirror noise.

Despite the additional noise contribution of the folded cascodes, this leads to overall better noise performance for the novel amplifier architecture. The emitter resistors of the standard topology cannot be made significantly larger without further circuit changes, as the current mirror output might become saturated under certain conditions.

Well-mannered overload behaviour is, particularly with more complex amplifier topologies, not always easily achieved. Typical artefacts include [2]:

- Polarity reversal during clipping
- Oscillation during, or during recovery from, clipping
- Prolonged recovery from clipping

Fortunately, the basic overload behavior of the novel amplifier topology is quite good; figure 14 depicts the output voltage of the model amplifier from figure 12 attempting to provide a 10 kHz, 4 V_{PP} triangle waveform output with $\pm 15\text{ V}$ power supplies. There is some prolonged recovery from clipping discernible, but no polarity reversal or instability.

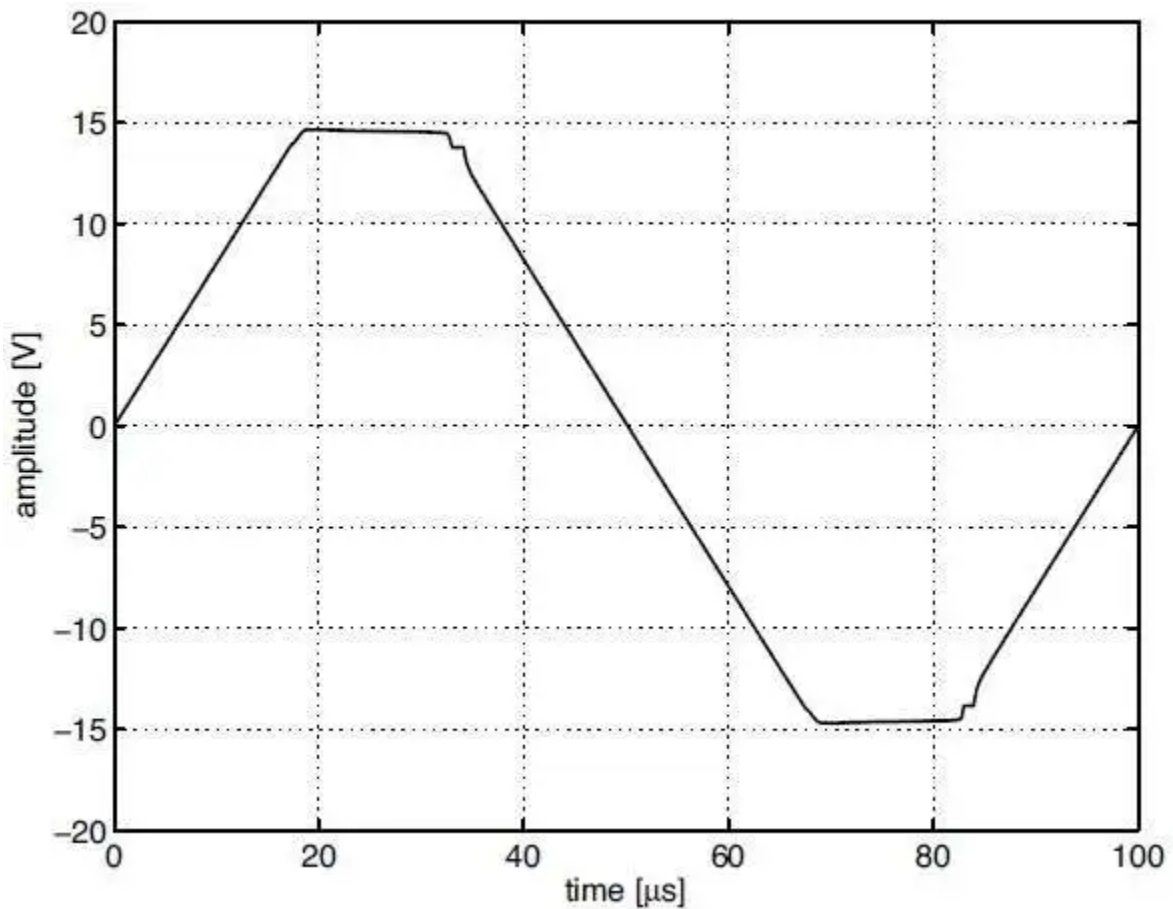


Figure 14: Overload behavior of the model amplifier from figure 12.

In contrast, the standard amplifier topology shows distinctly asymmetric overload behavior, and for negative clipping, considerable artifacts (see figure 15). While I do not believe that there are drastic audible differences between the overload behavior of the two amplifier topologies – last but not least, serious clipping sounds pretty bad anyway, and the observed artifacts occur in the μs range – an oscilloscope display similar to figure 14 will surely please a reviewer’s eyes much more than one close to figure 15.

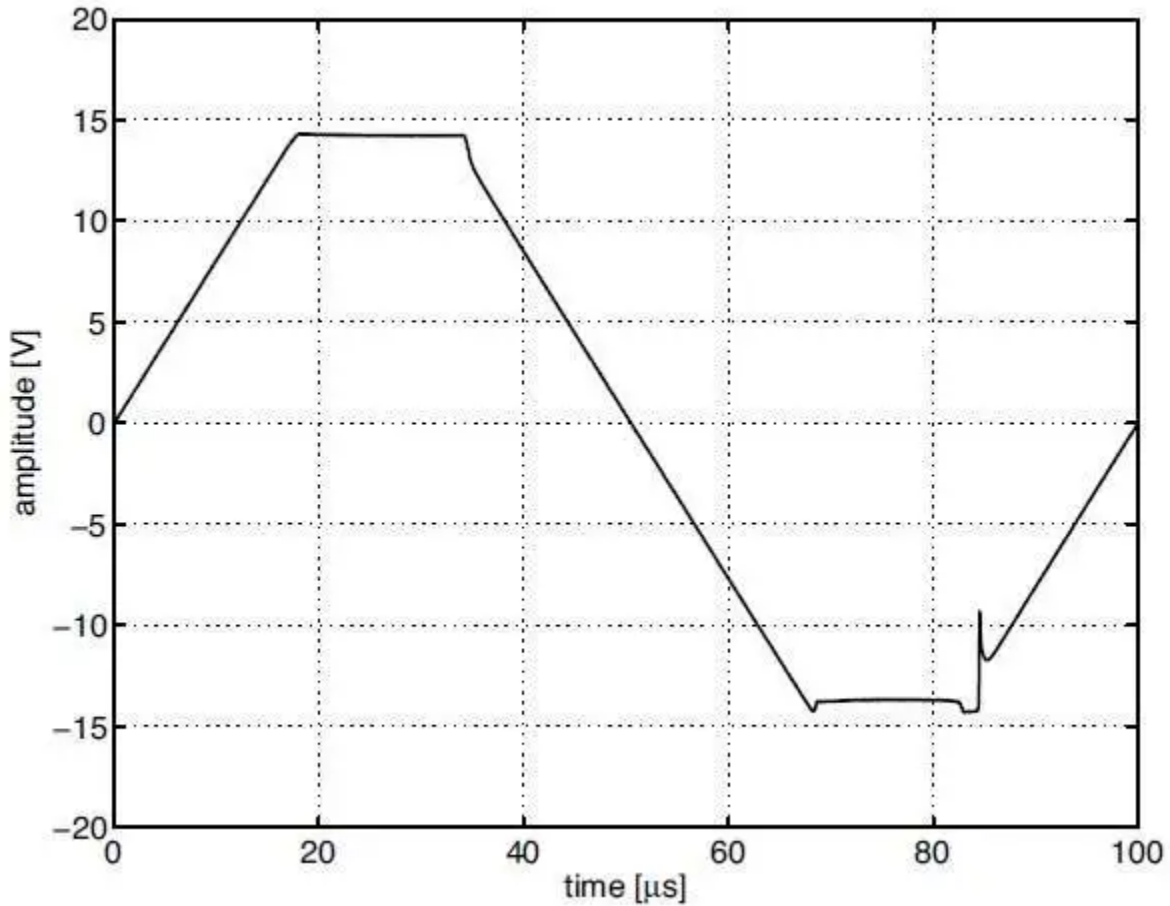


Figure 15: Overload behavior of the model amplifier using the standard amplifier topology.

These measurements neglect the contribution of the power transistors in the output buffer. Often these suffer themselves from considerable recovery time [2], and it may be desirable to prevent saturation of these transistors by clamping the output voltage of the transimpedance stage to a well-defined threshold below the power supply voltage. Implementation of such a clamping arrangement is often difficult, particularly because it must not impair the distortion performance of the amplifier below clipping. Some possible implementations may be found in [2].

As the model amplifier from figure 12 does not implement voltage regulators for the amplifier front end, and hence the potential power supply rejection advantage of the new topology is not fully realized, I have not carried out detailed power supply rejection measurements yet. Initial measurements however indicate that the main injection mechanism is indeed absent and that the model amplifier from figure 12 has – even without the voltage regulators – overall better power supply rejection than the standard amplifier implementation shown in figure 11.

Last but not least the slew rate of these two model amplifiers was evaluated. The measurement results were $+46.8 \text{ V}/\mu\text{s}$ and $-45.6 \text{ V}/\mu\text{s}$ for the standard topology and $+42.3 \text{ V}/\mu\text{s}$ and $-43.4 \text{ V}/\mu\text{s}$ for the novel amplifier. These results are mainly determined by the primary slew rate limitation (finite output current of the input

stage), which masked the expected advantage of the novel topology. The overall lower slew rate of the novel amplifier is probably just a result of parts tolerances, which lead to lower input stage quiescent current; possibly there is also a minor systematic effect from the input stage folded cascodes.

To also model the, at high frequencies potentially considerable, drive current demand of a power output stage, I've added a 3.3 k Ω resistor from the second stage output node to ground. This was sufficient to make the slew rate behavior of the standard topology more asymmetric (the measured values are +42.4 V/ μ s and -44.6 V/ μ s). The new push-pull configuration however easily supported the increased output current. The resulting slew rates are +41.4 V/ μ s and -42.6 V/ μ s, which is nearly the same as what is observed without the loading resistor.

To more thoroughly verify the absence of slew rate limitations in the second stage, I have also constructed a model amplifier based on the topology sketched in figure 8, using the input stage modifications derived in [8] and the very same second stage implementation as shown in figure 12. With a total input stage quiescent current of about 20 mA, and a compensation capacitor of 100 pF, the achieved slew rate was +226.6 V/ μ s and -228.3 V/ μ s. Additional loading at the transimpedance stage output altered this to just +223.5 V/ μ s and -222.4 V/ μ s.

This is enough evidence to conclude that the novel transimpedance stage indeed supports very high slew rates; simulation results indicate that, with appropriate changes to the input stage, much higher values are theoretically possible. However, the effects from finite small-signal bandwidth soon makes further efforts in this direction meaningless.

10. Conclusion

In this article, I have presented a new transimpedance topology, suitable for combination with a wide range of input stages to form amplifiers with two gain stages. Compared to prior amplifier designs, the novel architecture shows distinct advantages. First of all, it features inherently good power supply rejection, which is easily improved further by the use of voltage regulators for the amplifier front end. These voltage regulators are easily implemented at low cost and complexity.

The transient current output capability of the new transimpedance stage is considerably enhanced as well, and will easily support the design of amplifiers with a very high slew rate. This comes along with reduced sensitivity to loading at the second stage output node – this is a very welcome property, as it simplifies the design of the power output stage. Also, the clipping behaviour was shown to be superior to the standard amplifier topology. The novel second stage topology requires level shifting at the input stage via folded cascodes. I have outlined how their impact on offset and voltage noise can be minimized, and shown that the noise performance of an amplifier using the new transimpedance stage may even be superior to prior implementations; that is because of reduced current mirror noise contribution. There is a complexity penalty associated with the new circuits, compared to the standard amplifier implementation. However, there is no significant cost increase to be expected, as just small-signal transistors and standard passive components are needed. Also, the increased quiescent current is usually of no relevance within the context of a full power amplifier design. I must leave the design of a fully worked out power amplifier design, using the new concepts presented here, to future research. However, the interested reader will find it easy to derive his own

implementation from the presented model amplifier. If, as suggested in section 7, voltage regulators for the amplifier front-end are used, the design from figure 12 will only need minor modifications in the folded cascodes of the transimpedance stage to accept high voltage power supply rails. With the addition of a suitable power output buffer, and the necessary control and protection circuitry, a complete power amplifier is realised. To the best of my knowledge, this new amplifier topology is first officially published in this article. However, it is not possible to investigate all prior art, particularly all the information buried within the extensive patent repository. I shall be happy to hear about any findings with this respect from my valued readers. In Part 4: Appendix: Noise in folded cascode stages. **11. Acknowledgements**

I'm very grateful to Bob Cordell for reviewing this text and for providing valuable thoughts on it. I'd like to express my thanks to Jan Didden for his efforts in publishing this article and for providing us with an excellent resource on audio electronics. **References**

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Samuel Groner was born and currently lives in Zurich, Switzerland. He has been passionate about both art and science as long as he can remember. At present he works for Weiss Engineering Ltd. in the field of analogue hardware design and freelances as classical recording engineer/producer. Besides this, he teaches several courses at a local sound engineering school (ear training, classical music production and audio measurement) and enjoys a manifold activity as pianist, singer and choirmaster. If time permits, he is

found on one of the numerous Swiss hiking trails, preferably in company with one of his cameras and a few sheets of black-and-white film. He holds a MSc degree in computer science and a MA degree as Tonmeister (recording engineer/producer).

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