

Square law rules in **AUDIO POWER**

To the best of Ian Hegglun's knowledge, the difference of two squares concept has never been used in audio power amplifiers, but as this work shows, there are significant linearity benefits to reap.

Michael Williams' article [1] shows how the difference of two squares — D2S [Note¹] — produces a linear output from a pair of fets, forming the basis for a perfect linear amplifier. This approach has never been intentionally applied to class-AB amplifiers to reduce distortion [Note²]. The reason is probably the inherent difficulty in obtaining conjugate gain characteristics in the crossover region to prevent crossover distortion [2, 3].

Newly developed circuit techniques could solve this problem, and put the square-law to work in high power audio amplifiers. Experimental results demonstrate the effectiveness of these techniques, but first a look at the underlying theory.

Crossover distortion in class AB

Class-AB is most widely used due to efficiency and lower cost relative to class-A, but class-AB generates more distortion than class-A. Distortion from class AB is mainly crossover related and cannot be eliminated by trimming. Negative feedback has difficulty reducing crossover distortion in the high audio range, where there is generally less feedback available for distortion reduction [4] and our ears are more sensitive to frequencies (and hence distortion components) appearing in the 1-5kHz range [Note³].

The crossover distortion problem of class-AB power amplifiers is essentially that each of the two output devices must operate in two different modes. Firstly, each device must have constant gain at high currents, but secondly they must have a variable gain in the crossover region where both devices contribute to output current as is illustrated in **Figures 1a to 1f**.

The ideal transfer function for no distortion is of course a straight line, **Fig. 1a**. Gain is represented by the slope of the line which is constant, **Fig. 1b**. Both devices conduct in the crossover region between $-VI$ and $+VI$. The gain of each device must sum to a constant value in the crossover region and the total gain must also match the gain outside the crossover region.

¹ Footnote 1. I do not recommend using the 'D2S' abbreviation (coined by Michael Williams) since the abbreviation is already in use for a 'Differential-to-Single' (D2S) converter, also D2S is also a type of xenon lamp (HID), and again D2S is the commercial product name of a surround-sound receiver. I prefer to use the term 'Squarelaw differencing Class-A' — a deliberate choice for uniqueness. 'Square law' or 'Square-law' are correct spellings, but 'Squarelaw' is a deliberate misspelling for uniqueness. 'The difference of two squares' is also correct usage. The difference of two squares relationship giving a linear result is found in most mathematics encyclopaedias under the 'Quarter-Square' identity: $a \cdot b = 1/4 \{ (a+b)^2 - (a-b)^2 \}$. This was used in the 1960's to perform analog multiplication, with diode arrays performing the squaring. To use it in an electronic amplifier, simply make the term b a constant (the 'bias' voltage) and use fets to perform the squaring. A push-pull complementary pair of power mosfets can provide the difference of currents at the output node for direct drive to a loudspeaker load. To drive standard speakers some negative feedback is required to reduce the output resistance. This gives square-law class-A. Squarelaw class-AB is more tricky (see footnote below).

² Footnote 2. Michael Williams article only considers Squarelaw differencing in Class-A mode — where the mosfets are biased so both remain conducting over the full cycle at rated power. My article mainly considers Squarelaw differencing in Class-AB mode — where the mosfets are biased so one can turn off when the power level is high enough. In this mode simply reducing the bias of a Squarelaw differencing Class-A amplifier produces a lot of distortion at higher power levels due to an increasing gain at high power, referred to as 'bat-wing' gain rise by Doug Self (EW Oct 1995, p886-7). My two Squarelaw differencing Class-AB designs aim to minimise this effect.

³ Footnote 3. Fielder L, Benjamin E, 'Subwoofer performance for accurate reproduction of music', (JAES June 1988, p443-456) shows distortion the order of 0.0003% is detectable repeatably under certain test conditions. A similar acknowledgement comes from the recent adoption of 24 bit resolution and ultrasonic bandwidth of 96kHz (or higher) for audiophiles, see Robert Stuart, 'Coding for High-Resolution Audio Systems', JAES v25(3) March 2004, p117-144. Note 16 bit 44.1kHz CD format equates to about 0.002% THD at best, and is now acknowledged as inadequate for audiophiles, thus ending the 'Great Debate'. Not all 0.003% THD amplifiers sound the same (eg G Randy Slone www.zusaudio.com/technology/zusaudioengine.htm#THDvsF). For interesting reading on the 'Great Debate' see Robert Harley's 'The Listeners' Manifesto', Stereophile, January 1992 www.stereophile.com/reference/20/.

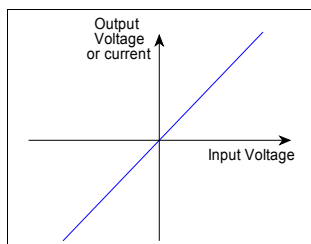


Fig. 1a) A straight line transfer function is required for no distortion.

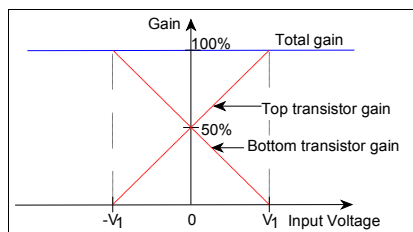


Fig. 1b) shows gain variation for a class-AB output stage. Voltage $-V_1$ to $+V_1$ is the crossover region. Individual gains in the crossover region need to sum to a constant value for no distortion.

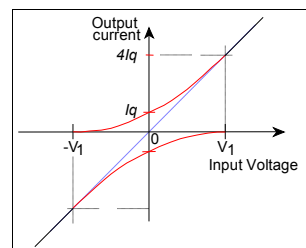


Fig. 1c) the transfer functions required for Fig. 1b are square-laws in the crossover region and linear beyond.

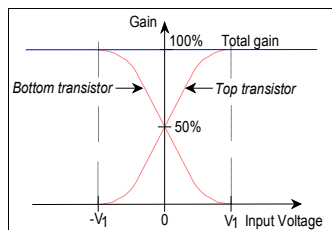


Fig. 1d) shows an alternative gain function that also gives no crossover distortion. Both curves must have conjugate gain symmetry.

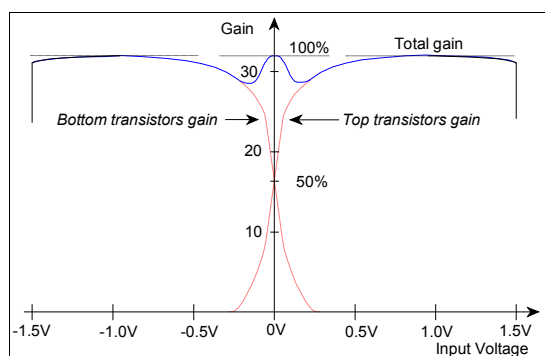


Fig. 1e), gain linearity of a bipolar common-emitter output stage is shown (based on Self's Fig. 8 Ref. 6). Asymmetry makes it impossible to eliminate distortion.

With symmetrical components, the gain of each device when V_{in} is zero must be exactly 50% for a sum of 100%. These requirements give a family of symmetrical gain functions that result in zero crossover distortion. A constant rate of change of gain, Fig. 1b, gives the square-law V-I transfer curve **Fig. 1c**. This can be found from the gain function by simply integrating a constant gain from $-V_1$ for the positive conducting device, and likewise integrating down from $+V_1$ for the other device.

An alternative gain function which satisfies the 50% gain requirement and is symmetrical about $V_{in}=0$ is shown in **Fig. 1d**. At low currents, fets show exponential deviation from square-law [5], resulting in a gain curve that is initially exponential. This gives a 'rounded' gain function at low currents, Fig. 1d [Note⁴]. This is fortuitous and suggests it may not be necessary for a fet to show perfect square-law characteristics at low currents to give perfect linearity, provided that the gain curve can be made symmetrical at the high current end. This should be possible somehow, by altering the shape of the top end transition, i.e. the region slightly below $+V_1$ for the +ve side device.

Unfortunately, classical class-B bipolar and classical class-B mosfet stages do not meet these requirements at optimum or any bias level. **Figure 1e** [6] shows significant gain non-linearity around the crossover region for an optimally biased class-B bipolar stage operating in common emitter, effectively the open-loop form of an emitter-follower stage.

In this example the mid-gain is 32 with a gain dip of -4 in the crossover region, representing a 13% change even when biased for minimum distortion.

⁴ Footnote 4. A look at the second derivative gives a symmetric bell-shaped curve, indicating the V-I transfer function changes from more than a square-law function at low currents, to a squarelaw at $V_{in}=0$, and then changes to linear at $+V_1$. In a typical class-B bipolar stage (Fig. 1e) gain change is approximately linear (i.e. square-law) over half the crossover region. In other words, class-B bipolar stages typically perform square-law differencing over half of their crossover region. So what's new in this article? Firstly, my two designs provide an order of magnitude better linearity than typical mosfet designs, secondly, they operate at a relatively high bias current to perform class-AB without gm-doubling or 'bat-wing' gain rise, thirdly, they do not have a transient bias displacement problem, and fourthly, in my second design (Fig. 6) the optimum bias point does not depend on load impedance. In short, two class-AB designs where the long-standing crossover distortion problems are overcome simply and economically — without resorting to pure class-A.

This gain error results from one transistor turning off too fast, before the other has reached constant gain. It is the resistors in the emitters of the power transistors that cause the gain to flatten at high currents, but the rate that the transition occurs is too slow and therefore over far too wide a range.

Figure 1f is the V - I transfer function for the same example (Fig. 1e) with a $\pm 1\text{V}$ input and therefore giving $+32\text{V}$ output and $+4\text{A}$ peak into an 8 ohm load.

The difference between a straight line of average gain, about 31, and the actual output trace is the distortion component. In this case the error voltage is about 500mV pk-pk, or 200mV rms, representing a total harmonic distortion (THD) of about 1%.

In most amplifiers this stage is configured as a unity-gain follower, and the action of local feedback, some 30dB , reduces the total harmonic distortion to 0.03% , and the addition of the usual $20\text{-}30\text{dB}$ of global feedback reduces THD to around 0.003% [Note⁵].

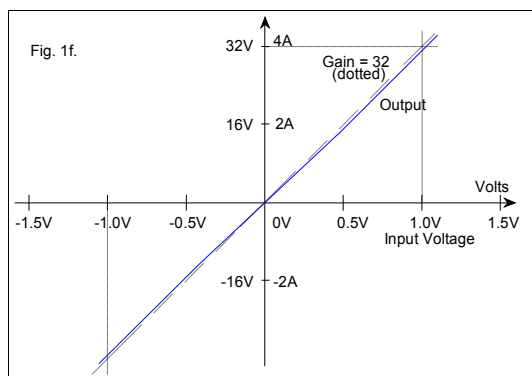


Fig. 1f shows the resulting transfer function for the bipolar common-emitter output stage (Fig. 1e). The difference between the average gain of 31 and the output is the distortion component, in this case about 1%.

More feedback

Negative feedback is usually used to reduce crossover distortion. But due to increasing phase change with frequency, a limit must be put on the amount of negative feedback [7]. In particular, the gain of the feedback loop plus the amplifier must be under unity at the frequency where 180° phase shift occurs. This prevents oscillation and likely destruction of the output transistors.

Load impedance variations have an effect on the loop gain-phase relationship. Capacitive loading from speaker leads and speakers adds phase shift to the output and therefore to the feedback signal [8]. Most output stages are unity-gain follower types with 100% local feedback. These are more sensitive to loading than output stages that have less than 100% feedback and hence a gain above unity. However, both require an appropriate Zobel network to overcome this instability problem [Note⁶].

Using fets as square-law devices, it should be possible to reduce the amounts of feedback required to a level that eliminates complications caused by loading—making amplifier design easier.

The ideal circuit should also be highly efficient—preferably as high as class AB—to minimise cost. Any distortion should consist mainly of a few low-order harmonics rather than the high order variety [9].

Our ears are more sensitive to high-order odd harmonics produced by crossover distortion—particularly if they lie in the sensitive hearing region. Ivor Brown suggests the multiplicity of high order harmonics from crossover distortion

⁵ Footnote 5. THD measurements correlate so poorly with what we hear that THD values are generally meaningless for audiophiles. Distortion measurements need to be weighted to correlate well—where higher order harmonics are multiplied by a suitable weighting factor and then summed to a total value, and Shorters $N^2/4$ weighting (from 1950) works well (see Keith Howard's 'Weighing up', Hi-Fi News March 2005, p78-81) suggesting our hearing is acutely sensitive to the second derivative or the rate-of-change of gain when the distortion products lie in the sensitive hearing range (1-5kHz). This is bad news for class-B amplifiers since class-B produces the most rapid gain changes (in the crossover region) compared to class-A. My simulations show the weighted-B distortion figure is 30-100 times higher than the THD figure. Even with typical global feedback levels most class-B amplifiers still produce audible distortion. Silicon Chip magazine was honest enough to print this in a reply to a letter 'Amplifier design philosophy questioned', (March 2004, p6), where SC said, "Indeed, high order harmonic products from [class-B] amplifiers can be heard at extremely low levels in quite ordinary loudspeakers. Our 15W class-A design from July 1998 has the lowest THD we have ever measured [$\sim 0.0003\%$]. It is also the best sounding amplifier we have ever heard—the clarity has to be heard to be appreciated. On that basis alone, we feel justified in always striving for the very best THD performance".

⁶ Footnote 6. Even before global feedback is added an emitter-follower (EF) output stage can oscillate when capacitively loaded, due to frequency dependent negative resistance generated at HF by negative feedback, making the EF a prospective oscillator when driving a capacitive load. See de Lange (Dewald), Flat, Wideband Buffers, EW Oct 2003 p199-203; Eric Margan 'Amplifier Instability', EW April 1998, p311-312; Millman-Halkias 'Integrated Electronics' Sec. 11-10 p369-370; Choma J, 'Output inductance of an emitter follower', IEE Electronic CAS, July 1997, p162-4. Oscillation can be prevented by adding input resistance (gate-stopper or base resistors) and adding a 'Zobel' RC series network which lowers the output stage gm at HF. Output stages with less than 100% local feedback (eg the 'current feedback' stage like my Fig 2) are less likely to oscillate before applying global feedback. However, output stages with less than 100% local feedback are more likely to oscillate with global feedback when driving a relatively large capacitive load when phase advance is used (applied from the load)—see the debate Cherry vs. Gift (JAES, May 1982, p295-305) and 'Feedback amplifier output stages' (JAES Oct. 1985, p787-800). A better compensation scheme than the standard Miller type that suits such output stages was found by John Linsley Hood (Letters WW Sep 1973 p449-450) and used in his 'chokeless' designs (eg WW Jun 1982 p40-42). This has also been the subject of recent research for CMOS opamps which use common-source output stages (not source-followers) to obtain wider output voltage swings. The CFP is undesirable for class-B (but not class-A) because the 100% CFP feedback narrower crossover current range (than the darlington EF or an output stages with gain), giving higher order harmonic distortion at lower power levels, both are undesirable for audio, and this makes it even harder for global feedback to make crossover distortion inaudible.

reduces spatial definition [10] [also see footnote 3].

Differencing two squares

Michael Williams's article [1] explains the principle of subtracting or 'differencing two squares' or 'D2S' as he called it, or alternatively 'Curvilinear class-A', since paradoxically, this linearity is derived from nonlinearity.

By definition, squarelaw differencing is class-A, since both devices are always conducting. Linearity can only be obtained with squarelaw differencing over the limited input voltage range of $-V_1$ to $+V_1$ as shown in Fig. 1b and Fig. 1c.

However, the mode of operation shown in Fig. 1c is class-AB — a different class from D2S, which I call 'Square-law class-AB'. In this mode only one device conducts when the input swing exceeds $+V_1$. This mode improves efficiency and reduces the amount of heatsink required, but makes it hard to obtain good linearity at high currents. This is the aim of my present square-law Class-AB designs.

As Williams points out, squarelaw differencing has the advantage of a lower quiescent current than conventional class-A per output watt. Heat dissipated at idle (P_q) with squarelaw differencing is $1/2 I_{pk} V_{cc}$, since the quiescent current is set at a quarter of the peak output current ($I_q = I_{pk}/4$) and not half I_{pk} as for conventional class-A.

For split supply rails of $\pm V_{cc}$, quiescent power dissipation P_q is $2V_{cc}I_q$, which is $1/2 I_{pk} V_{cc}$. Neglecting saturation and ripple voltages, this is the same as the output power rating, or $P_q \sim P_{out}$ for squarelaw differencing.

Saturation and ripple voltages, say 2 volts for saturation and 2 volts rms of ripple (6 V_{pk-pk}), which increases dissipation by about 10%. Both conventional class-A and squarelaw differencing class-A require this same margin, this means a practical class-A push-pull amplifier will dissipate twice the power of the squarelaw differencing class-A amplifier per output watt.

The maximum possible sinewave efficiency for squarelaw differencing class-A, as detailed in the panel [Efficiency in squarelaw differencing Class-A](#), is 66.7% [Note⁷], compared to 50% for conventional push-pull class-A and 78.5% for class-B. For class-B, dissipation peaks at approximately half full-power, dissipating typically the same amount as heat. As a result, maximum dissipation is 1/2 of maximum output power, so squarelaw differencing class-A must dissipate no more than 2.5 the power of class-B (in practical designs it is slightly under twice).

By operating in squarelaw differencing class-A crossover distortion can be avoided completely and at little extra cost. Distortion components due to mosfets not obeying a true square-law and mismatching are mainly second and third harmonics.

Most of the second harmonic can be trimmed by equalising the gain difference, and there are a wide variety of options for error correcting the third harmonic distortion caused by the gain-drop of the mosfets.

Trimming these errors could be considered a form of *feed-forward* error correction, where the effectiveness rests on the stability of the various parameters to maintain a distortion null after the set-up phase. Most amplifiers already require the setting of one preset at manufacture, so another should not be a serious disadvantage.

Implementing the concept

Douglas Self [6] explored a power-fet square-law circuit (Self's Fig. 2) but found the range for the square-law only extended over a disappointing 80mA range of output current. This circuit was class-AB with only one device conducting at high currents.

Examining the V-I transfer curves of Self's Fig. 10, you can see that considerable local feedback is applied to the fets by adding the source degeneration resistors. About 1 volt appears across the 0.22 ohm source resistors at 5 A with 1.5 V input. This amount of feedback kills the square-law relationship— even at low currents. Reducing or eliminating these resistors would increase the useful square-law current range.

The design example described in the panel [A 100W squarelaw differencing Class-A fet amplifier](#) shows that IRF540/9540 vertical power mosfets could achieve squarelaw differencing class-A power levels of 100W with distortion as low as 0.0005%, and that without any trimming. This appears possible even with a 12% fet gain drop at peaks, and a 16% mismatch. It shows ultra low distortion squarelaw differencing amplifiers are not only possible but cheaper than conventional class-A amplifiers [Note⁸].

⁷ Footnote 7. My original article calculated the efficiency wrongly. The error was in the last line of the derivation, a simple fraction manipulation. This corrected article also includes an alternative derivation, to confirm that the analysis is correct. Further analysis is added for the dissipation and power supply requirements along with a summary table for conventional class-A and class-B. My original article stated D2S (squarelaw differencing Class-A) must dissipate twice the power of class-B, but strictly speaking it should have been 2.5 times using my updated analysis. In practical designs it is slightly under 2 times that of class-B. Incidentally, a comparison with conventional Class-AB and square-law class-AB modes is due to be published soon.

⁸ Footnote 8. My original article said I wasn't aware of anyone deliberately making use of the square-law principle in a commercial design, either in class-A or class-AB. But within a year of publishing I discovered that the 'SuperMos' amplifier by Les Sage was 'efficient class-A' (eg advertisement 'Supermos 2' in Elektor Electronics, Feb 1990, p72). It used mosfets with no source degeneration — the method needed to achieve squarelaw Class-A in practice. His design achieved remarkably low distortion as predicted here. Sadly, production appears to have stopped and he never received proper recognition for his revolutionary designs. I for one would be very interested in viewing his circuit diagram.

Bengt Olsson's designs in 'Better Audio from non-complements?', (EW+WW, Dec. 1994, p988-992) uses squarelaw differencing but was improperly assessed by Douglas Self's article 'Few compliments for non-complements', (EW+WW Sept 1995, p762-5) in Fig. 6 where the mosfet plot appears to be wrongly normalised. A subsequent letter by Bengt Olsson (Oct 1995, p886-7) revealed that the distortion of the output stage alone measured 0.02%; which incidentally is the distortion calculated in my panel A 100W squarelaw differencing Class-A fet amplifier. Bengt Olsson mentioned higher efficiency with the lower $R_{ds(on)}$ of vertical mosfets, but he did not

Class AB square-law circuits

The circuit of **Fig. 2** was constructed to evaluate power fets for class-AB. It is similar to Self's Fig. 2 evaluation circuit [6], minus the source resistors. Since lateral mosfets are used, source degeneration resistors are not needed to prevent thermal runaway.

Driver transistors Tr3,4 provide level shifting for the mosfets, as well as biasing and some voltage gain. Unlike conventional class-AB driver circuits the emitters are not coupled. This gives a wider crossover region— slightly wider than the fets' range $\pm V_1$.

The power fets effectively operate open-loop, being common drain with no source resistors. An optional small amount of voltage feedback is used to trim the high-current gain for symmetry to minimise second harmonic distortion at high power levels.

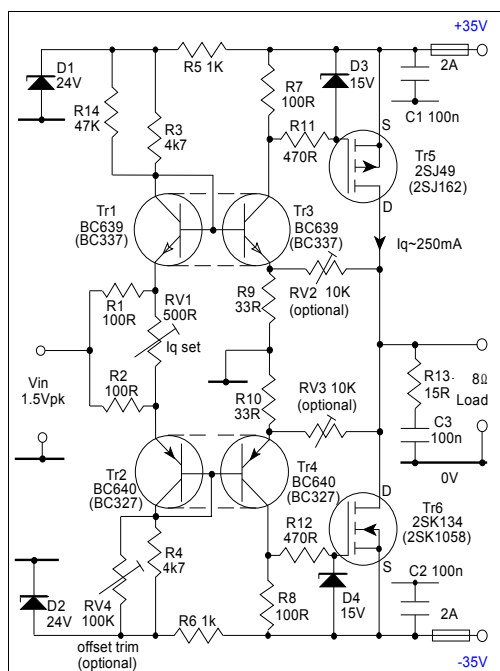


Fig. 2. Class AB output stage with power fets operating as approximate square-law devices in the crossover region with correction provided by increasing gain of the driver transistors.

Figure 3 shows triangle wave input and output voltages with an 8 ohm load. The supply voltage has been reduced to +22V so saturation can be seen, showing good open-loop linearity up to within a few volts of saturation and soft clipping. Note traces are offset by 0.47 volts to aid viewing and set-up trimming. The vertical differences represent the output error voltage. A deviation of about 0.2Vpk-pk appears at the ends, covering about 1/4 of the time, allowing the rms error voltage to be estimated from these traces without a distortion meter. Since total harmonic distortion is the ratio of rms error voltage to rms output voltage, the rms error voltage can be calculated using:

$$V_{rms} = V_{pk-pk} / (2 \sqrt{2}) \times \sqrt{t/T} \text{ where } t/T \text{ is the duty cycle.}$$

provide efficiency measurements, had he done so he would have observed the reduction in heat arising from this square-law class-A mode. Audiophiles could now be enjoying squarelaw class-A along with lots of money saved, but very few seem to have cottoned on 10 years after several practical circuits appeared in print.

You may be wondering why I didn't make it clear in my original publication that Bengt Olsson's design was a practical squarelaw differencing amplifier, ie revolutionary. My article was undergoing the final stages for publication when Bengt Olsson's design appeared in the New Zealand bookshops. It wasn't until the October issue the following year that he made it clear that he was using squarelaw differencing. Anthony Holton is one person exploiting Olsson's output stage www.ausieamplifiers.com.

Another example of a square-law differencing—the 'MJ amp' (MJ Stereo Technique, Japan, 1995. www.homestead.com/whaan/files/index.html, or search "MJ amplifier"). It was designed to operate in class-A with no source resistors and uses lateral mosfets with a gain driver-shifter (strikingly similar to my Fig. 2 design, arrived at independently). But I suspect efficiency was not measured. Conventional class-A cannot achieve more than 50% efficiency but square-law class-A can. Since my original article I have built many similar lateral mosfet class-A amplifiers, and have obtained 52% with 50W into 8 ohms with lateral mosfets, and with error correction (to give a more ideal square-law) I got 56%. See the *Summary Table* under the panel *Efficiency in squarelaw differencing class-A* — the maths says it works, and it really works— really.

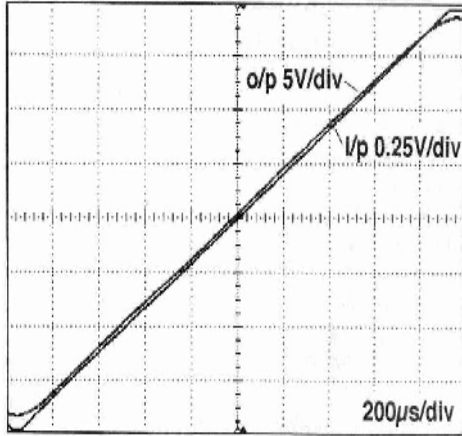


Fig. 3. Output of circuit of Fig. 2 with a triangle wave input shown for comparison.

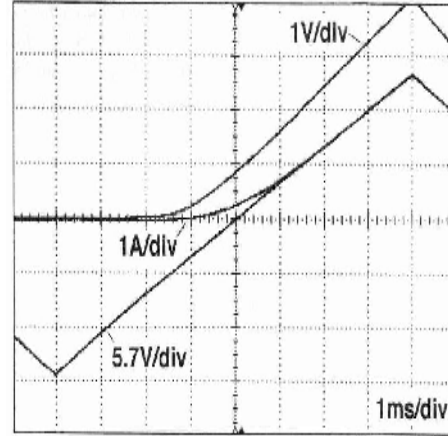


Fig. 4. Curves for Fig. 2 with output voltage, Tr3 current and gate voltage show square-law region, linear region and non-linear gain of driver used to compensate for fet gain drop.

In this case error voltage is 35mVrms for 12Vrms output voltage, giving 0.3% THD for this output stage which is essentially operating in open-loop. More open loop measurements are shown in **Table 1**.

Table 1. Open-loop performance of amplifier Fig. 2

Phase shift was 180° at 10MHz with 8 ohm load.

Load [ohms]	Bias [mA]	THD [%]	Gain [V/V]
8.0	250	0.8	20
4.0	500	0.5	15
8.0	500	0.5	30

The Hitachi lateral mosfets used here have a 7A and 140V rating and an RDSon of 1 ohm (1.5 ohms at 100 C). Measurement showed their gate thresholds were very low (0.3V) and hence the quiescent voltage across gate bias resistors R7,8 were only 1.1V and -0.75V respectively for the optimum quiescent current of 250mA for 8 ohm loads.

Although these mosfets are relatively high on-resistance compared to modern vertical power mosfets, they are still capable of delivering high currents efficiently in this design since gate voltages can swing up to 2/3 of the supply voltage, and hence need to be limited by zeners to under 20V to prevent the mosfets from being damaged. For a low saturation voltage of say 3V, the fets need to be restricted to 3 amp peak or 50 Wrms output, although linearity is still good up to 5A allowing speaker impedance dips of typical speakers to be safely handled, making lateral mosfets cost effective.

[panel] **Efficiency in squarelaw differencing class-A**

Equations in this panel describe efficiency in squarelaw differencing class-A using two square-laws.

With a sinewave signal $V = k \sin \omega t$ where k ranges from 0 to 1, the top half has a current waveform given by.

$I_{D1} \cong \frac{1}{4} I_m (1 + k \sin \omega t)^2$ where $I_m = V_{dd}/R_L$ and $I_q = I_m/4$ for a square-law amplifier. The bottom half is

$|I_{D2}| \cong \frac{1}{4} I_m (1 - k \sin \omega t)^2$. First find the average current for the top half

$$I_{Dave} = \frac{1}{\pi} \int_{-\frac{\pi}{2}}^{+\frac{\pi}{2}} \frac{1}{4} I_m (1 + k \sin \omega t)^2 d\omega t$$

$$I_{Dave} = \frac{1}{4\pi} I_m \int_{-\frac{\pi}{2}}^{+\frac{\pi}{2}} (1 + 2k \sin \omega t + k^2 \sin^2 \omega t) d\omega t$$

$$I_{Dave} = \frac{1}{4\pi} I_m \int_{-\frac{\pi}{2}}^{+\frac{\pi}{2}} \left(1 + 2k \sin \omega t + \frac{1}{2} k^2 (1 - \cos 2\omega t) \right) d\omega t$$

$$I_{Dave} = \frac{1}{4\pi} I_m \left[\omega t - 2k \cos \omega t + \frac{1}{2} k^2 \left(x - \frac{1}{2} \sin 2\omega t \right) \right]_{-\frac{\pi}{2}}^{+\frac{\pi}{2}}$$

$$I_{Dave} = \frac{1}{4\pi} I_m \left(\pi + \frac{\pi}{2} k^2 \right)$$

$$I_{Dave} = \frac{1}{4} I_m \left(1 + \frac{1}{2} k^2 \right)$$

By symmetry $P_{INave} = 2V_{dd}I_{ave} = \frac{1}{2}\left(1 + \frac{1}{2}k^2\right)V_{dd}I_m$

so $P_{OUTave} = \frac{1}{2}V_{pk}I_{pk} = \frac{1}{2}kV_{dd} \times kI_m = \frac{1}{2}k^2V_{dd}I_m$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\frac{1}{2}k^2V_{dd}I_m}{\frac{1}{2}\left(1 + \frac{1}{2}k^2\right)V_{dd}I_m} = \frac{k^2}{1 + \frac{1}{2}k^2}$$

Maximum possible sinewave efficiency is 2/3 or 66.7%. With lateral mosfets for 50W into 8 ohms $V_{sat} + V_{ripple} \sim 5V$ and hence $V_{cc}=35V$, then $k=0.88$ and maximum sinewave efficiency is 56%.

An alternative method

$$I_{D1} \cong \frac{1}{4}I_m(1 + k \sin \omega t)^2 = \frac{1}{4}I_m(1 + 2k \sin \omega t + k^2 \sin^2 \omega t)$$

$$V_{DS1} = V_{dd}(1 - k \sin \omega t)^2 \text{ and so } P_{1ave} \cong V_{DS1}I_{D1} = \frac{1}{4}\left(1 - \frac{1}{2}k^2\right)V_{dd}I_m$$

Due to symmetry $P_{1ave} = P_{2ave}$ so $P_{DISave} = \frac{1}{2}\left(1 - \frac{1}{2}k^2\right)V_{dd}I_m$. Also $P_{OUT} = \frac{1}{2}k^2V_{dd}I_m$

$$\text{so } \eta_{Sq-A} = \frac{P_{OUT}}{P_{OUT} + P_{DIS}} = \frac{\frac{1}{2}k^2V_{dd}I_m}{\frac{1}{2}k^2V_{dd}I_m + \frac{1}{2}\left(1 - \frac{1}{2}k^2\right)V_{dd}I_m} = \frac{k^2}{k^2 + 1 - \frac{1}{2}k^2}$$

Hence $\eta_{Sq-A} = \frac{k^2}{1 + \frac{1}{2}k^2}$ and again we find maximum efficiency is 2/3 or 66.7%.

Other important parameters are Input power (P_{in}) and Power dissipated (P_{dis}), both expressed as a fraction of maximum theoretical rms output power ($P_{out max}$), they are found by:

$$P_{DISave} = P_{OUTave} - P_{INave} = \frac{1}{2}k^2V_{dd}I_m - \frac{1}{2}\left(1 + \frac{1}{2}k^2\right)V_{dd}I_m = \frac{1}{2}\left(1 - \frac{1}{2}k^2\right)V_{dd}I_m$$

so P_{in} as a fraction of maximum theoretical rms output power ($P_{out max}$) is given by:

$$\frac{P_{INave}}{P_{OUTmax}} = \frac{\frac{1}{2}\left(1 + \frac{1}{2}k^2\right)V_{dd}I_m}{\frac{1}{2} \cdot 1^2 V_{dd}I_m} = 1 + \frac{1}{2}k^2 \text{ For } k=1 \text{ max. input power is } 1.5P_{out max}.$$

$$\text{Also } \frac{P_{DISave}}{P_{OUTmax}} = \frac{\frac{1}{2}\left(1 - \frac{1}{2}k^2\right)V_{dd}I_m}{\frac{1}{2} \cdot 1^2 V_{dd}I_m} = 1 - \frac{1}{2}k^2$$

Min. dissipation is $0.5 \times P_{out max}$. Worst case dissipation is $P_{dis} = 2 V_{dd} \times I_q = 1/2 V_{dd} \times I_m = P_{out max}$.

Table 2. Summary Table for 3 classes

Parameter	Classic-A	Square-law-A†	Class-B
Eff (k)	$1/k^2$	$k^2/(1+0.5k^2)$	$\pi/4$
Max Eff	50%	66.7%	78.5%
Practical max Eff*	45%	62%	75%
$P_{in}(k)/P_{out max}$	2.0	$(1+0.5k^2)$	$4k/\pi$
Worst case $P_{in}/P_{out max}$	2.0	1.5	1.27
Practical worst P_{in} *	2.0	1.45	1.30
$P_{dissipated}/P_{out max}$	$2(1-0.5k^2)$	$(1-0.5k^2)$	$4k/\pi - k^2$
Quiescent dissipation	2.0	1.0	0
$P_{dissipated}/P_{out max}$	1.0	0.5	$2/\pi \sim 0.57$
Worst case $P_{dis}/P_{out max}$	2.0	1.0	$(2/\pi)^2 \sim 0.40$
Practical worst P_{dis} *	1.1	0.55	0.31

† Assumes true square-law devices. Actual mosfets deviate from square-law and this moves practical values closer to Classic-A.

* Practical case assumes $k = 0.95$, for a 50W/8R amplifier mosfets with an $R_{ds on}$ of 0.25 ohms can achieve this.

A 100W squarelaw differencing Class-A fet amplifier

For 100W continuous into 8 ohms, output swing is $\pm 40V$ peak and $\pm 5A$ peak. For squarelaw differencing Class-A, quiescent current must be set at $1/4 I_{pk}$, or 1.25A. Peak input voltage V_1 can be calculated for a specified distortion level as follows. Mobility modulation [5] causes a reduction in output current at high current, causing deviation from the theoretical square-law relationship.

Assuming matched fets, there is no second harmonic, but there is mostly third harmonic distortion for which, $D_3=1/24 (D_+ + D_-)$ (eq. 12 of ref. [11]). With mobility modulation, $I_d(q)=b(V_g-V_t)^2/(1+q(V_g-V_t))$, where b is beta (the transconductance constant), V_g is gate voltage, V_t is threshold voltage, and q is the mobility reduction factor (theta in Symbol font).

Taking the ratio of current with mobility modulation to the ideal current gives $I_d(q)/I_d(ideal)=1-q(V_g-V_t)$. This shows the gain compression factor $A \sim q/(V_g-V_t)$. For, say, 1% of third-harmonic at full power using the equation for D_3 , with $D_+=D_-$, gives $DG=0.12$. Using a typical value for q of 0.1 (1/V), peak gate

rise VG-VT is 1V. This means that Vin is ± 0.5 Vpk. With a 3V threshold voltage, the fets would need to be biased at 4V, reducing by $-6\text{mV}/^\circ\text{C}$. Since peak current is 5A with a gate rise of 1V, the fet requires a gain of 5A/V. For an IRF540, data sheet V-I transfer curves by plotting $\text{Sqrt}(I_d)$ against VG using, slope = $\text{Sqrt}(b/2)$. This yields a b of $11\text{A}/\text{V}^2$ with VT at 3V for both IRF540 and IRF640's.

Their complements, the IRF9540 and 9640, typically have betas that are 25% lower. This means they are suitable for a 100W square-law differencing Class-A class-A amplifier with 1% THD open loop.

Fet gain mismatch causes the gains at each end to be different, giving mainly second harmonic distortion, calculated from, $D_2 = 1/8 (D_+ - D_-)$ (eq. 12a of ref. 11). A mismatch of 8% adds 1% second harmonic distortion. Total open loop distortion is 1.4%, $D_{\text{tot}} = \text{Sqrt}(D_2^2 + D_3^2)$

Open-loop voltage gain is calculated from $A_v = G_{fs} \times R_L = 80$ where the overall gain G_{fs} is calculated above at the end points. Distortion of this output stage can be compared to other unity gain output stages using the relationship, $DCL = DOL / (1 + BA_{OL})$ where B is 1 for 100% feedback.

With a gain of 80 and 1.4% open loop distortion, the equivalent unity gain distortion is 0.02%. Similarly, a gain drop of 20% with a gain of 80 is equivalent to a drop of 0.3% at 70% output swing at 30W, giving 0.0012% THD at 20kHz with 30dB global feedback factor, also at 20kHz. [End]

To measure fet current, a 0.1 ohm sensing resistor was temporarily placed in the supply rail. In this position there is no noticeable effect on linearity. **Figure 4** shows fet current with output voltage using a triangle wave input after trimming for best linearity. The output voltage plot is vernier scaled so the curve merges with the current trace. This allows both the square-law and linear regions to be clearly seen in the top half, similar to the curves shown in Fig. 1c.

The gate voltage is also displayed at 1V/div (more below). The current waveform appears to be a square-law within the crossover region and outside the gain it is reasonably linear. The square-law crossover region covers an input swing of $\pm 0.8\text{V}$. The quiescent current of 220mA was stable with temperature on a $1^\circ\text{C}/\text{W}$ heatsink. Current at the end of crossover region is about 0.8A — four times I_q — indicating square-law operation within the crossover region.

The gain of the driver transistor can be measured from the gate voltage waveform. It doubles from $-V_I$ to $+V_I$. Increasing the gain of the driver transistors offsets the mosfet's gain drop (due mainly to mobility modulation) within the square-law region, resulting in a near ideal square-law-like relationship. At V_I the fet has essentially gone linear, demonstrating that power mosfets can be made to follow a gain plot like that of Fig. 1d which allows highly linear class-AB operation as well as high efficiency [Note⁹].

Values of $R_{7,8}$ were altered to suit the amount of compensation required for a particular fet and operating current range. Increasing bias voltage gives less gain compensation for higher gate bias voltages of modern power fets. I expect equations can be found to calculate resistor values from the SPICE mosfet model parameters [Note¹⁰].

It appears that the slow gain change of the bipolar class-AB circuits — which is the cause of crossover distortion — is advantageous in off-setting the slow gain change of the fets from square-law to linear.

Modern opamps with output swings of $\pm 10\text{V}$ can be used to drive this type of output stages because it provides useful voltage gain. For example, the *OPA627*, although expensive, can give distortion figures as low as 0.0003% [12] with a gain of 3 and the *NE5534* can give almost as good performance [13] at lower cost.

Modern opamps can provide suitable slew rates, and more importantly, reduce component count. They are probably not more widely used in this type of application because the usual starting point in a design is a voltage follower, unity gain, output stage.

Other advantages of using this type of output stages with gain are:

- Improved output stage stability due to lower feedback factor.
- Higher efficiency due to lower saturation voltage.
- Biasing current can be derived from a lower voltage regulated and filtered supply.
- Improved power supply rejection and reduced power rail intermodulation distortion.
- Slew rate for the driving amplifier is reduced by the factor of the output stage gain.
- Driver transistors only need to be rated at half the supply voltage.
- Output is a current source, current limiting can be performed by simply limiting input voltage swing using diodes.

Another square-law circuit

The circuit of **Fig. 5** the driver for the bipolar power transistors uses a 'composite pair' comprising Tr9,10 (from a 74HCU04 cmos inverter) and Tr3,4 which provides some advantages such as even better linearity and stability with temperature than my power mosfet output stage Fig.2. In this arrangement ambient temperature variations do not affect linearity, and linearity is insensitive to load resistance changes (as was found with Fig. 2 in Table 1).

⁹ Footnote 9. The main feature of my circuits for square-law operation is that gm-doubling or 'bat-wing' distortion is essentially eliminated, while still operating at a relatively high optimum bias current — essentially implementing John Linsley Hood's class-A/AB concept (see Wireless-World, June 1970, p278-280; and E&WW, March 1989, p259-264) — which offers the best world of high efficiency and a wide class-A power band that spans several watts — and is therefore ideal for audiophile use since there is no high order distortion, even at very high power levels.

¹⁰ Footnote 10. The section of analysis on gain peaking was omitted since I found it to be wrong in general since it was based on an approximate formula for G_{fs} . I had only checked it with a BUK546 at publication but later simulations with accurate models showed that it was necessary to use electrothermal power mosfet models as well as driver transistors to obtain useful information and to obtain similar waveforms to those reported here.

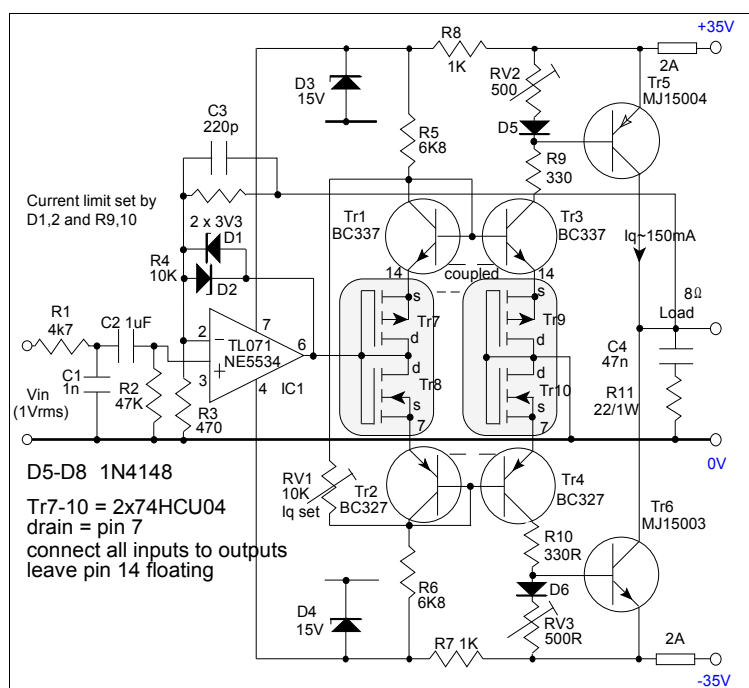


Fig. 5. *This class AB amplifier uses complementary mosfets in the emitters of the drivers to give accurate square-law current differencing in the crossover region and a linear gain outside the crossover region by making use of the bipolar's beta-fall at high currents.*

Cmos inverters provide well matched complementary fets that readily available and low cost. When the six inverters in a HCU04 are paralleled, 120mA can be safely handled. At 120mA the gain drops by only 10% and this amount of current is sufficient to drive a bipolar power transistor to 5A output, given a typical beta of 50 at 5A.

Six HCU04 inverters in parallel give parameters $b=50\text{mA/V}^2$, $V_T=0.8\text{V}$ and $q=0.12\text{ (1/V)}$. Matching of p- and n-gains (beta values) was within a few percent for devices with the same date mark. The threshold voltages of p-fets were typically 80mV higher than n-fets.

Figure 6a shows an improvement allowing lower crossover distortion by using all n-fets, thereby obtaining better matching. Here Tr7,9 act as virtual complements. Transistors Tr3,4 act as voltage followers and transfer the input voltage to the gates of Tr9,10, and then the resulting mosfet currents are level shifted up to the output transistors by Tr3,4. Here the mosfets, and not the bipolar drivers, determine the gain and crossover region. The HCU04 package voltage is varied for optimum linearity over the crossover region with RV1.

Gain matching of each half is achieved with RV2,3 in series with small signal diodes D5,6. This method is very effective, allowing large gain variations between individual bipolar transistor pairs, as well as making use of the beta-fall in the bipolar transistors at high currents beyond the crossover region (above 1A) to overcome the usual gain rise or 'batwing' effect with mosfets beyond the crossover region.

In conventional bipolar output stages a base-emitter resistor is usually employed to remove base leakage current to speed up their turn off time and thereby minimise the troublesome common mode current increase at high frequencies which can destroy the output transistors if high frequency oscillation at full power occurs. But in Fig. 6 these resistors are cannot be used since they would cause unacceptable non-linear gain in the crossover region. High frequency (fast) power transistors can be used to prevent this.

Since no base-emitter resistors are used, thermal run-away is prevented by adding temperature sensing diodes D7,8 in **Fig. 6b** which are soldered to a lug under the TO-3 bolt to the case of Tr5,6; which is a more economic option than using a larger heatsink. With suitably high-gain transistors ($\beta>300$) across the base-emitter terminals of Tr5,6 the temperature-dependent leakage current can be drained away without upsetting linearity, thereby prevent thermal run-away and allowing a minimal heatsink.

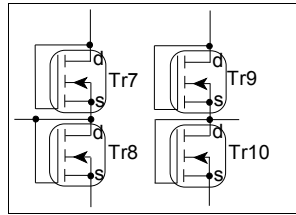


Fig. 6a) Alternative arrangement for Tr7,10 giving significantly better matching and lower crossover distortion. Note transistors Tr7,8 are virtual complements. Use four 74HCU04's for Tr7-Tr10; source is pin 7, leave pin 14 floating.

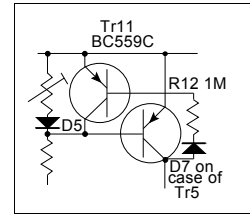


Fig. 6b) Collector-base leakage current compensation prevents thermal runaway in Tr5. A similar circuit (not shown) is used for Tr6

In Fig. 5, mosfets Tr7,8 are used as a temperature related bias voltage generator for the active mosfets. Quiescent current through Tr7,8 is mirrored into Tr9,10 independent of ambient temperature changes. The dynamic resistance of the bias generator pair Tr7,8 is small compared to R5,6, being $1/gfs$ where gfs is $\text{Sqrt}(2bId)$, or around 100 ohms (since Id is 1 mA). At this current the HCU04 package develops around 5 volt and this voltage is trimmed for optimum linearity over the crossover region using RV1.

With a low impedance voltage source for a drive there is little incremental drop across this bias generator as the input voltage varies. Since the input voltage swing is only +2V, resistors (R5,6) can be used rather than active current sources to set the bias current.

Power supply ripple rejection from the auxiliary supply 15V supply rails is about 30dB, and the zeners D3,4 providing another 30dB from the main power supply rails.

Resistors R9,10 in the collectors of Tr3,4 limit the output current during output-shorts and this limiting also prevents secondary breakdown in the output transistors. With a V_{ce} of 50V (the worst case for $\pm 35V$ rails) the ISB rating for these transistors is 4A.

Resistors R9,10 are calculated by assuming a beta of 50 at 4A for the power transistors Tr5,6. Peak base current is therefore 80mA, so 30V across R9,10 requires 330 ohm resistors. These resistors conveniently also reduce power dissipation and hence electrothermal memory in the drivers Tr3,4. Free-standing TO-92 devices were acceptable for my 50 watt version, but higher power versions will need MJE340/350's (or equivalent) on a small heatsink. Transistors Tr5,6 which were MJ15003/4's measured gains of 110 and 80 respectively at 1A, both falling to 50 at 5A. MJ15003/4s were used mainly because of availability. Higher frequency power transistors ($FT > 5\text{MHz}$) are recommended in higher power applications (more below).

Optimum bias was achieved at around 150mA with a total bias voltage of 1.7V in Fig. 5 made up of 785mV across n-channel fet Tr8 and 863mV across the p-channel fet Tr9 — a difference of some 83mV due mainly to mosfet threshold mismatch. This difference was found to cause one side to finish its square-law before the other, which gives a non-linearities near the ends of the crossover region which could not be trimmed out by any means.

However, using all n-channel fets for Tr8,9 (as in Fig. 6a) the bias voltages match to within 6mV allowing non-linearity in the crossover region to now be removed by trimming the quiescent current. Distortion at 500Hz was 0.3% when the swing reached 60% of the full output. Most of the harmonics were third and fifth order.

Voltage gain was 13 with an 8 ohm resistive load. Full power bandwidth was 70kHz, and gain-bandwidth product 1MHz.

With the modification of Fig. 6a total harmonic distortion after trimming by a factor of 3 to 0.1 % at 500Hz. **Figure 7** shows the open-loop transfer curve. There was only a slight temperature induced change in linearity, observed between idle and running continuously at maximum power [Note¹¹].

¹¹ Footnote 11. Stable biasing is very important. Keith Howard's 'Bias assessment,' (Hi-Fi News, October 2004, 84-9) provides weighted distortion tests on two amplifiers starting from cold and found one example so bad that he said, "expletive-deleted". Previously no reviewer has ever included bias compensation tests in any of their reviews, but Keith Howard mentions that "some reviewers monitor it informally". He appears to be the first to use weighted distortion measurements to look at transient class-B distortion, which is due to a biasing error between the output transistors and the bias voltage generator, which is thermally coupled to the output transistors but time delayed. A sudden temperature change in the output transistors throws out the biasing for about a minute until the sensor catches up; in this period you may get gross crossover distortion. The worst case scenario is a quiet period immediately after a sustained loud period of music. Keith Howard's results indicate that there is a real need for accurate temperature compensation for class-B output stages. Douglas Self mentioned the problem (Part 6, E & WW, Jan 1994, p41-45), and developed better designs (see Douglas Self's 'Thermal dynamics in audio power,' EW May 1996, p410-415) and more recently the Tag McLaren 700:7r.

My hunch is that bias displacement error has never in the past been measured because designers would have to admit that they haven't a simple solution to this problem, and admitting this would mean abandoning class-B designs in favour of either class-AB (which develops high gm-doubling distortion), or class-A, which in conventional designs is prohibitively expensive for all but a few.

Sanken developed a special pair of power transistors to overcome this problem, the SAP15/16, which integrates a diode into the power transistor die. I note they are used in Music Fidelity's kW 500 (Hi-Fi News, October 2004, p20-3). Sanken's data sheet claims there is a noticeable sonic improvement, but no distortion measurements (as at late 2005). Mosfets are inherently less sensitive to junction temperature changes (see Robert Cordell's 'A mosfet power amplifier with error correction', J. AES, Jan/Feb 1984, p2-16). He says, "Compared to bipolar designs, class-AB mosfet power output stages tend to have a wider class-A region of operation (because of their higher bias current) and a smoother transition to the class-A region" — which is very significant to our hearing because of lower-order harmonics.

These characteristics are probably the reason why, over the last 30 years, that mosfet class-AB amplifiers were generally found to sound more pleasant than bipolar class-B amplifiers. Hitachi lateral power mosfets were designed for audio amplifiers with the unique property of a temperature stable bias point at around 100mA, so a bias loop

Load impedance changes did not have any noticeable effect on linearity. This contrasts with the power mosfet version Fig. 2 optimum bias depends on loading. In Fig. 5 optimum bias was not affected by load resistance.

Tests were done with the collector-base leakage compensation Fig. 6b disabled [Note¹²]. The quiescent current through the output transistors increases from 150mA (set for optimum bias) to 230mA immediately following a run at full power for some time. Interestingly, this variation does not affect linearity.

One problem observed using bipolar output transistors that was not observed in power mosfet output stage was asymmetric switching distortion which generated high levels of second harmonic distortion at the top end of the audio frequency range. It can also be seen on an oscilloscope as differences in the bandwidth of the output transistors, in this case it reached a maximum of 3% at 10kHz and 33V pk-pk, first noticeable at 2kHz, and at 5kHz it rose to 1%.

Since the negative half of the amplifier generally has the higher gain and is the lower bandwidth half, a 10R resistor with a shunt 1uF speed-up capacitor can be added in series with the emitter of Tr4. Over the audio range the bandwidth can be made the same and second harmonic distortion in open-loop can be made comparable to the earlier power mosfet circuit Fig. 2. Of course in closed-loop arrangement with global feedback the power mosfet circuit achieves much lower distortion levels due to its higher bandwidth.

Circuit Fig. 6a has demonstrated that a stable 0.1% THD can be achieved up to 2kHz open loop with a gain of 13 using readily available non-selected parts. Closed-loop distortion could not be measured with the HP54601A using FFT. Closed loop THD however is expected to be 0.001% at 1kHz and 0.006% at 20kHz. This assumes an TL071 providing about 40dB feedback at 20kHz.

In closed loop, C3 provides some phase advance above 70kHz — the output stage roll-off point— keeping the loop phase less than 180° until the gain has fallen below unity.

Using similar transistors in a complementary feedback-pair output stage, Self's Fig. 8 class-AB amplifier of reference 2 shows distortion reaching 0.01% at 20kHz, using a 37dB feedback factor at 20kHz. This he attributes mainly to crossover and switching distortion.

But with a 37dB feedback factor, output stage distortion can be calculated to be 0.7% with optimal biasing — 50 times higher than the 0.014% expected from an optimally biased complementary-feedback pair [14]. Presumably the 0.7% figure is mostly due to switching distortion and not component mismatch. Note, the emitter resistors only affect gain match at high current — not the transistors.

My power mosfet output stage is expected to give 0.001% THD at 20kHz; as mentioned its higher gain and wider bandwidth can allow a higher feedback factor at 20kHz [Note¹³].

My power mosfet output stage is also expected to match the class-A design of 0.0012% at 20kHz by Self [4, 10] with a similar spread of low order harmonics.

Setting optimum bias

I developed a straightforward technique for setting optimum biasing using an oscilloscope and triangle wave source. The alignment is carried out with an open loop by connecting a 100uF capacitor across D1 which simply disables global feedback. Trimming is best achieved at about 50% of the maximum output swing by applying about 1.5V peak triangle wave with an 8 ohm resistive load.

Display the input and output waveforms together, as Fig. 3. Set RV1 at zero and RV2,3 at maximum. Raise quiescent current to about 150mA then determine which half shows the lowest slope. If, for example, the lower half has the lower gain then vary RV1 for best linearity— lower half only. Lastly, reduce RV2 until the upper half has the same slope as the lower half. The overall line should then be straight.

Better things yet to come?

It is pleasing to see fets go linear at higher currents in a way that allows near elimination of Class-AB crossover distortion. Two different techniques have demonstrated that class-A performance is possible using class-AB— one circuit using power fets over their full current range, and the other using fets driving bipolar power transistors.

is not required and there is no long term bias displacement distortion. Although the THD measurements of lateral mosfet class-AB amplifiers are generally higher than bipolar amplifiers, their harmonics when weighted come out way ahead of bipolars in class-B at the normal power range for listening (see footnote 3).

12 Footnote 12. At the time of testing I assumed that thermal runaway would occur due to junction temperature rise in the bipolar output transistors like other output stages so I included the additional transistors of Fig. 6B, but to check this I disabled them for this test. To my surprise and delight thermal runaway did not occur and is not needed. Furthermore the slight increase in quiescent current corresponded to the bias level for minimum distortion at the higher junction temperature. This was later found to be due to the output transistors being operated as current driven devices and not voltage driven (since base-emitter resistor was used) and in this current drive mode the collector current is not an exponential relationship with junction temperature but instead the gain (beta or Hfe) increases by only about 50% for a 50C junction rise.

13 Footnote 13. But to drive highly capacitive loads and some types of speakers and some speaker cables an *output choke* must be added for stability. But this restricts the bandwidth, and recent findings confirm the need for an ultrasonic bandwidth throughout to preserve transient wavefronts to prevent 'time-smearing'. Mike Story in 'A suggested explanation for (some of) the audible differences between high sample rate and conventional sample rate material', (www.dcsltd.co.uk file AES.PDF, Sept 1997, pp5) said, "A simple explanation of audible differences introduced by CD audio is the impulse response of the anti-alias filters (for CD) spread the transient information over a much longer time - so the audio picture is 'defocused' ... the energy in the ringing can be large (-9dB or 12%) of the main lobe. To stop this energy defocusing a Gaussian filter (no ringing) and -1dB at 20 kHz for -120dB at fs/2 requires an fs of 440kHz, however an fs of 192kHz and its slight ringing may be acceptable for no audible defocusing. CD at 44kHz spreads the ringing over 1ms or more (to -60dB), while 192kHz brings it to within 50us (20 times lower) almost as good as a Gaussian (analog) filter. Interestingly, even oldies with significant high frequency loss say the spatial localisation of 96 and 192 is very much better than 44.1. ... hence multichannel audio needs the higher sample rate to provide its aim of better spatial localisation of sound sources!"

Whereas the bipolar output-stages low bandwidth degrades performance above 2kHz, the power fet output stage is free from switching distortion and can allow more feedback at the top audio end giving superior overall performance.

My tests showed that class-AB crossover and high-current distortion can be reduced to 0.1% in open loop using simple techniques — a factor of 10 better than conventional class-B stages. In the future it may be possible to achieve a further order of magnitude improvement, or two orders of magnitude lower open loop distortion using integration techniques, such as integrating Tr1-4 and Tr7-10 on the same chip. Integration also allows automatic biasing using master-slave circuit techniques [16] to monitor linearity and correct any changes [Note¹⁴].

These fet based circuits demonstrate that class-A performance need not be traded for class-AB efficiency.

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End of original article

This version includes corrections (see list below) and footnote explanations which discuss developments since the original publication.

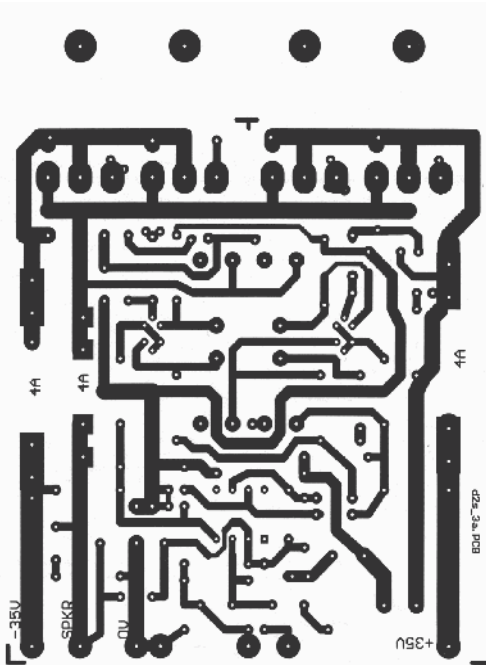
¹⁴ Footnote 14. See Adams W, Ramirez-Angulo J, 'Extended transconductance adjustment/linearisation technique', (Electronics Letters vol. 27 no. 10 May 1991, p842-844) which utilises square-law differencing and a master-slave self calibration and temperature correction to form a programmable linear transconductor element.

Corrections: 1. The paragraph on stability in *More Feedback* removed. 2. In Table 1—frequency 10MHz. Paradoxical meaning of 'Curvilinear class-A' added. 3. The maxim possible sinewave efficiency changed to 66.7%. Also corrected in the panel on 'Efficiency in squarelaw differencing Class-A'. (More analysis added and summary table to compare classic-A, squarelaw differencing Class-A, and Class-B.) 4. squarelaw differencing Class-A must dissipate 2.5 times the power of class-B (originally twice), but practical designs it is slightly under 2 times. 5. Sentence added to *Class AB square-law circuits*—with lateral mosfets thermal runaway is not possible with no source resistors. 6. Para. for *Figure 3*, added 'soft clipping'. 7. R_{DSon} is 1 ohm rising to about 1.5 ohms at 100 C. 8. Changed '100W average into 8 ohms' to 'linearity is still good up to 5A allowing speaker impedance dips of typical speakers to be safely handled' since it is not recommended that a pair of these mosfets should be used for 100W into 8 ohms due to typical speaker impedance dips well below 8 ohms with some down to 3.3 ohms. 9. 'Mosfet's gain drop is due mainly to mobility modulation', not it is due to velocity saturation in power mosfets—also changed in design panel for 100W squarelaw differencing Class-A. 10. In the section *Another square-law circuit* on Fig. 5 added comment that the bipolar drivers and cmos fets form a 'composite pair' hybrid transistor, and also clarifies my original intent that linearity is insensitive to load resistance changes unlike Fig. 2. 11. Deleted para. 'The HCU04 runs from 5V ...'. 12. Changed para. on diodes D5.6. Added clarification about gain rise (ie batwing effect) of power mosfets beyond the crossover region. 14. Changed para. on base-emitter resistor adding reference to common mode current which increases at high frequencies which can destroy the output transistors, and faster bipolar transistors which are now widely available are therefore recommended. 15. Para. removed on Tr3.4 voltage followers (covered better by modifying the first par of this section). 16. Para. on calculating R9,10 added reference to higher power version using MJE340/350's on a small heatsink to minimise electrothermal distortion (applies to Fig. 2 also). 17. Removed 3 para's about the digital meter static tests, since linearity changes at higher frequencies due to electrothermal or self-heating effects. 18. Switching distortion now as 2 separate paragraphs to better explain my original intent. 19. *Better things yet to come and conclusion* sections combined (removed reference to static tests). Added Fig. 5 gives a factor of 10 improvement in linearity. Reference 15 not now mentioned in the text. 20. Ref 14 corrected 'Part 4'. 21. Footnote 1 added and the abbreviation 'D2S' changed to 'squarelaw differencing Class-A' in the text (except for reference to Michael William's usage) since D2S is used in the literature is already used for a different technique (differential to single-ended conversion).

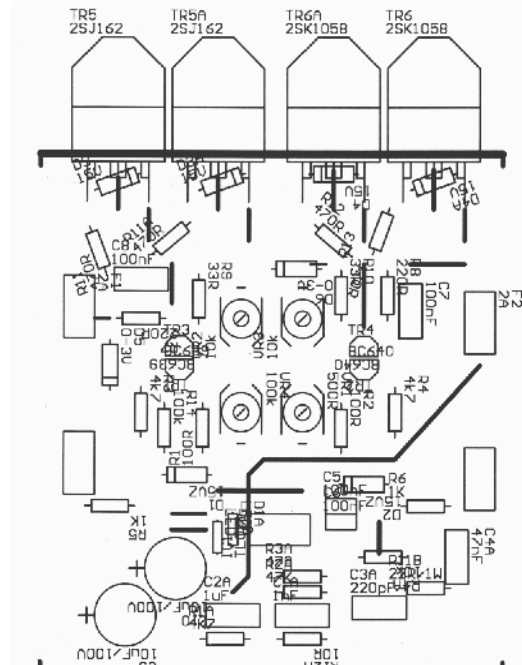
Keywords: Square law rules, square-law, squarelaw class-A, perfect linearity, low distortion, audio power amplifier, pure class A, class AB, class-A/AB, class B, high efficiency class A, squarelaw class-A efficiency analysis, negative feedback, stability, crossover distortion, optimum bias, conjugate gain function, Hitachi lateral mosfet, high bias class-AB with ultra-low crossover distortion, power output stage with voltage gain, eliminating the output inductor, common emitter, common source, voltage follower, composite pairs, virtual complements, electrothermal gain variation, load invariant linearity, low bias displacement error, ultrasonic bandwidth for audio, weighted harmonic distortion, master-slave biasing.

Related Keywords Difference of two squares, D2S, Curvilinear amplifier, class-A, class-AB, class-B, 56% record breaking class-A efficiency, 56% efficient class-A, bipolar audio power amplifier, mosfet audio power amplifier, output choke, symmetrical complement, low transient crossover distortion, low memory distortion, Les Sage SuperMos, Olsson Class-A, MJ amplifier, MJ-amp, Musen to Jikken Stereo Technique, 24 bit audio, CD audio quality, Douglas Self, Bengt Olsson, quasi-complementary, non-complement.

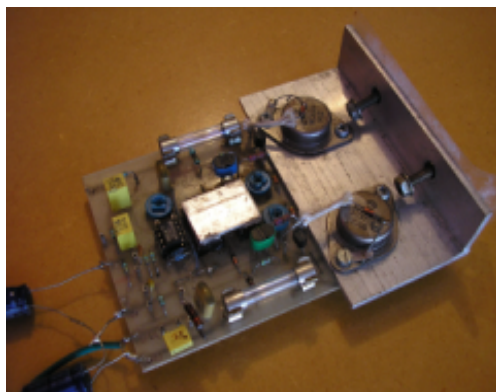
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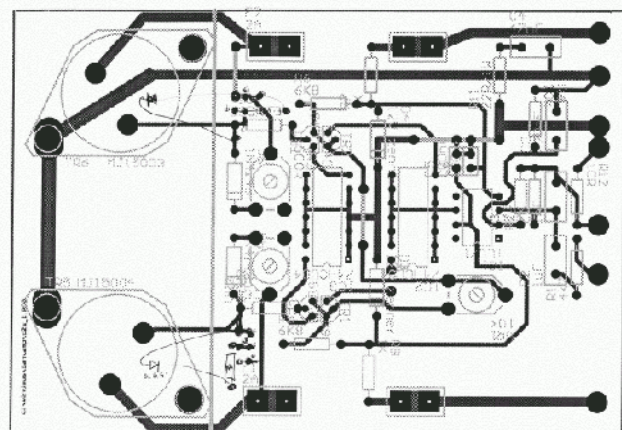
PCB for prototype 100W Mosfet Square-law Class-AB, Fig. 2 with parallel output mosfets.
Use $\pm 45V$ supplies for 100W into 8 Ω .



PCB overlay for prototype 100W Mosfet Square-law Class-AB.



Prototype 50W Bipolar Square-law Class-AB, Fig. 5. The 10R//1uF speed-up capacitor for Tr4 is top left corner.



PCB for prototype 50W Bipolar Square-law Class-AB. The 10R//1uF speed-up capacitor for Tr4 not shown.

Further technical references on the theory and application of the difference of square-laws.

1. **Hauser (Max W)**, Eric A.M. Klumperink, Robert G Meyer, William D. Mack, 'Variable-Gain, Variable-transconductance, and Multiplication Techniques: A Survey', in p291-322 (Chapter in Sansen (Willy), Huijsing (Johan H), van de Plassche (Rudy J), Editors, 'Analog Circuit Design: MOST RF Circuits, Sigma-Delta Converters, and Translinear Circuits', Kluwer Academic Publishers, 1996). The 1979 two-MOSFET squaring core of Seriki and Newcomb [ref 63] was proposed for quarter-square multiplication, a venerable analog-computer technique exploiting the algebraic identity $1/4\{(a+b)^2 - (a-b)^2\} = a.b$. Four main current difference techniques are reviewed, plus the source coupled pair with tail current linearisation, etc. In saturation FET's have $g_m \sim V_{gs}$ excess above V_{th} , but FET circuits are not as inherently accurate as the counterpart model for bipolar transistors, ...especially modulation of carrier mobility. For high frequency applications only a few methods can be used due to 50R and low noise requirements. There are 45 references on square-law difference applications (refs 63-108 see [Supplemental References](#) end of this section).
2. **Carruthers J**, Evans J, Kinsler J, Williams P, 'Linear c.m.o.s. circuits', WW Jan 1976, p75. Feb 76, p83. Circards 27,28: DC, AC amplifiers, gain controlled amplifiers, controlled resistances, square-triangle generator, two integrator oscillator, LP, HP, Notch filters.
3. **Smith R. D.**, 'Voltage follower with adjustable zero-offset', WW April 1980, p90. Complementary j-fets probably operate in square-law mode— good linearity & simple.
4. **Seevinck E**, Wassenaar R, 'A versatile CMOS linear transconductor/squarelaw function circuit', IEEE JSSC, vol. SC-22 no. 3 June 1987, p366-377. Analysis of 'linear' square-law class-AB 'is probably a unique capability' to $4I_q$ with no saturation at higher currents. With composite pairs no matching is required.
5. **Bult K**, Wallinga H, 'A class of analog CMOS circuits based on the square-law characteristics of an MOS transistor in saturation', IEEE JSSC June 1987, p357-365. Thd analysis and measurements.
6. **Park C**, Schaumann S, 'A High Frequency CMOS Linear Transconductance Element', IEEE T.CAS, Nov 1986, p1132-38. Cmos inverter as composite pair improves PSR, body effect distortion analysis. Fig 6 Clever linearised OTA structure and dc offset.
7. **Tarim T**, Ismail M, 'Robust design of low power cmos analogue integrated circuits,' IEE Proc Circ Dev Syst, Vol 148, No 4, Aug 2001, p197-204. New square-law composite cell, differential OTA and multiplier, statistical analysis.
8. **Filho S. N**, Schneider M. C, Robert R.N.G, 'New CMOS linear OTA circuit using square-law of mosfet', Electron. Lett. vol. 25 no. 24, 23 Nov 1989, p1674-5. Voltage biased source coupled pair (VCSCP) as Seevinck (1987), Szczepanski (1993), Schaeffer (1998) plus cfb correction. THD < 0.25% for 1Vpkin.
9. **Ramirez-Angulo J**, et al, 'Applications of composite BiCMOS transistors', ISCAS 1992, p1262-65. Composite pairs, application overview.
10. **Gaiulo G**, Maloberti F, Palmissano G, Portaluri S, 'Video cmos power buffer with extended linearity,' IEEE JSSC July 1993, p845-848. Dual cmos inverter input stages each with mirror to sum outputs— square-law differencing and p/n mismatch reduced. Related to CCII.
11. **Elwan H**, 'A low voltage cmos Class-AB operational transconductance amplifier', IEEE ISCAS 1999, pII-632-635. Seevinck implementation square-law class-AB input stage. Allows low current, low voltage, fast settling, linear at low currents. Good example of square-law principle.
12. **Ramirez-Angulo J**, 'A master-slave scheme to tune gain of transconductance amplifier with high accuracy', IEEE ISCAS 1993, p1176-9. Uses an identical master fed by V_{ref} in feedback loop to obtain the required bias for the main OTA. Makes it temperature independent, preserves band-width and eliminates offset and drift.
13. **Wunderlich R**, Oehm J, Dollberg A, Schumacher K, 'A linear operational transconductance amplifier with automatic offset cancellation and transconductance calibration', IEEE J.SSC 1999, p1321-4. 'Proposed idea uses the square-law principle for linearity' automatic 3 phase: offset nulling, then g_m calibration, then continuous-time filter.
14. **Shaeffer D**, et al, 'A 115-mW, 0.5-um CMOS GPS Receiver with Wide Dynamic-Range Active Filters', IEEE J. SSC Dec 1998, p2219-2231. Square-law Class-A using positive current feedback for error correction (makes mosfets closer to a square-law).
15. **van Zeijl Paul**, et al, 'A bluetooth radio in 0.18-um CMOS,' IEEE J. SSC, Dec 2003, p1679-1687.
16. **Giustolisi G**, Palmisano G, Pennisi S, 'High-linear class-AB transconductor for high-frequency applications', ISCAS May 28-31, 2000, pV-169-172. Square-law cell with gates connected to drains and cascoded to a mirror load similar to my Fig 5 (bjt version). Flat gain to 2GHz. A comparison with a LTP shows square-law is more linear.

17. **Ramirez-Angulo J**, Treece K, 'A second generation linear low voltage BiCMOS OTA', IEEE ICAS 1993, p1172-1175. Simulated structures: Multiple outputs, constant bandwidth input stage. Both square law differencing & LTP forms.
18. **Sevenhans J**, Paemel M, 'Novel CMOS Linear OTA using feedback control on common source node', Elect. Lett. vol. 27 no. 20 26 Sept 1991, p1873-1875. Why avoid using square-law difference (LTP— more dynamic range— high psrr).
19. **Wong L**, '1.8V low voltage pseudo-differential input operational amplifier', IEEE ISCAS 2002, pI-317-320. Unity gain inverting stage summed currents relies on matching for cmr, achieves 40dB cmrr, 80dB Aol, 350kHz Ft, 55uW. Small size.
20. **Nauta B**, 'A CMOS transconductance-C filter technique for very high frequencies', IEEE JSSC Feb 1992, p142-153. Balanced integrators with go cancellation cancel common mode parasitic caps, bw limited only by transit times (poles in GHz range) and matching accuracy. Square-law differencing with simple cmos inverters results in compact layout and tuneable by Vdd. 5% mismatch allows dc gain of 200
21. **Nauta B**, Seevinck E, 'Linear CMOS transconductance element for VHF filters', El Let vol. 25 no. 7 Mar 1989, p447-450. Square-law differencing using CD4049 tests CA3600/CD7007. Thd 0.05% 0.9Vpk with 8V supply, linearity plots.
22. **Kawahito S**, Tadokoro Y, 'CMOS class-AB current mirrors for precision current-mode analog-signal-processing elements', IEEE TCAS-II Dec 1996, p843-5. Cascoded mirrors and square-law differencing. Square-law Class-AB mirror gives lower sensitivity to mismatch than class-A current mirror.
23. **van-der-Heijden**, Mark & de-Graaff, Henk , et al, 'Theory and design of an ultra-linear Square-Law Approximated LDMOS Power Amplifier in Class-AB Operation', IEEE T. MTTs Sept 2002, p2176-84. Linearity and efficiency is better than conventional Class-AB or Class-A. (Downloadable free)
24. **Gajadharsing** (John R), 'Low distortion RF-LDMOS power transistor for wireless communications base station applications', IEEE MTT-S Digest 2003?, p1563-6. Companion paper to Heijden's Sept 2002 design. On production of a distributed Vth in a subdivided/paralleled power mosfet chip for 30W at 2GHz. Note— operation in the square-law region is called "class-AB" by this writer.
25. **Delle Curti** (Roberto), Speaker Damping Factor approximately unity (by drain pull-up resistors). www.royaldevice.com/custom3.htm. This rare mosfet power amplifier design uses no negative feedback— not even local feedback. It makes use of the difference of two (approximate) square laws to obtain good linearity with true zero-feedback. Note — a high Damping Factor is not needed since horn loading is used.

Multipliers using square-laws:

26. **Han G-H**, Sanchez-Senencio E, 'CMOS transconductance multipliers: A tutorial', IEEE T.CAS-II, Dec 1998, p1550-63. 70 refs as Gilbert, Linear, Saturation, Weak inversion, Current mode, others.
27. **Wang Z**, 'A CMOS four-quadrant analog multiplier with single ended voltage output and improved temperature performance,' IEEE JSSC vol. SC-26 no. 9 Sept. 1991, p1293-1301. Square-law differencing cell, a modified LTP with a voltage follower for Vbias (means inputs can float). Eg, a MOS resistor using square-law difference with temperature compensation. Uses two n-fets with gates direct to drains like my Fig. 2.
28. **Seng V, Rofail S**, 'Design and analysis of a $\pm 1V$ cmos four-quadrant analog multiplier', IEE Proc. Circuits, Dev. & Syst, June 1998, p148-154. Uses $\frac{1}{2}\{(a+b)^2 - a^2 - b^2\} = a \times b$ for good linearity at low voltage. BiCMOS used for less distortion and more bandwidth. This alternative square-law identity could be called the "half-square" identity. An alternative squarelaw amplifier can be made by making a (or b) a constant bias. It is not well suited for class-A power amplifiers since it only provides squarelaw class-A to $\pm 2I_q$ (not $\pm 4I_q$). It can be used for class-AB in a modified form where a resistor is placed across one mosfet to supply the bias current, permitting half the dissipation in the heatsink and giving asymmetric gm and asymmetric clipping and possibly desirable even plus odd harmonic distortion.
29. **Bult K**, Wallinga H, 'A CMOS Four-Quadrant Analog Multiplier', IEEE JSSC June 1986, 430-435. First simple multiplier using mosfets square-law. THD 0.14%. Square-law distortion analysis includes effect of channel length modulation and mobility modulation. Different all nmos V/I converter and is cascaded.
30. **Mavor J**, 'Analog CCD correlator using monolithic MOST multipliers', Electron Lett. 1977, p373-4.
31. **Hsaio S-Y**, Wu C-Y, 'A parallel structure for cmos four-quadrant analog multipliers and its application to a 2-GHz RF downconversion mixer', IEEE JSSC June 1998, p859-869. Uses square-law summing and differencing (6 cells). Good analysis of the effect of mobility modulation and length modulation. Main nonlinearity is from mismatching (since 2002 triple-well mosfets permit fast p's and better matching).
32. **Gilbert B**, 'A precise four-quadrant multiplier with subnanosecond response', IEEE J. of SSC Dec 1968, p365-373. Uses difference of squares called the 'quarter square' technique.

33. **Sakurai S**, Ismail M, 'A CMOS Square-Law Programmable Floating Resistor', IEEE ICAS 93, p1184-87. Drain connected to gate in a 'Seevinck Gm cell' — input is also output.
34. **Yamaji T**, Kanou N, Itakura T, 'A temperature-stable CMOS variable-gain amplifier with 80-dB linearly controlled gain range', IEEE JSSC May 2002, p553-7. Square-law amp input stages, exponential region end stages with master-slave control.

Opamps and Compensation:

35. **Palumbo G**, Pennisi S, 'Current-feedback amplifiers versus voltage feedback amplifiers', IEEE T.CAS-I May 2001, p617-623. CFB approach offers higher bw but lower AOL. The reported improvement by CFB opamps was probably due to a process changes at that time & not an inherent adv.
36. **Smith (Doug)**, Koen M (Burr-B), Witulski A, 'Evolution of High-Speed Operational Amplifier Architectures', Oct 1994, p1166-79. A VFB opamp input with LTP differential input stage generated 20dB more 3rd HD than a CFB input stage (operates in class-AB) for the same geometry & current, etc.
37. **Palumbo G**, Pennisi S, 'Design methodology and advances in nested-Miller compensation,' IEEE TCAS— I, July 2002, p893-903. 3 stages, CMOS AB output requires zero removal (due to common source output stages). With a resistor for zero removal large CL can be driven without ringing.
38. **Mita R**, Palumbo, G, Pennisi S, 'Reversed nested Miller compensation with current follower', IEEE ISCAS 2001, I-308-311. RNMC uses follower to stop feedthrough of i/p to o/p (hf zeros). GBW is not affected much by CL (good), provides better gbw than standard Miller compensation.
39. **Leung K-N**, Mok P, Ki W-H, Sin J, 'Three-Stage large capacitive load amplifier with damping-factor-control frequency compensation', IEEE JSSC Feb 2000, p221-230. Compared to single stage the gbw products of 2 (3) stage NMC are half (quarter). DFC halves chip area, 10 times GBW of Standard Miller and 10 times GBW of Nested Miller, Phase-margin is less sensitive to CL and useful for low power opamps. See Leung 2001 comparisons.
40. **Leung K**, Mok P, 'Analysis of multistage amplifier-frequency compensation', IEEE ISCAS 2001, p1041-1056. Compares 3 nested Gm-C 3 stage compensation with forward Gm stages. Only Damping Factor Control (DFCFC) is better for large CL, GBW falls as $\sqrt{CL}$, others fall as CL.
41. **Leung K-N**, Mok P, Ki W-H, Sin J, 'Analysis of an alternative structure of damping-factor-control frequency compensation', IEEE ISCAS 2000, pII-545-8. Called DFC2 by moving damping node back one stage (to output of first stage) — gives similar stability with CL but increases chip area and power. Similar to IEEE JSSC Feb 2000, p221-230.
42. **Kaulberg T**, 'A cmos current-mode operational amplifier,' IEEE JSSC July 1993, p849-852. Class-A (or AB) Two CCII's can provide differential input— uses square-law differencing. A 3rd CCII can provide a differential output.
43. **Lotfi R**, Shoaie O, 'A low-voltage low-power fast-settling operational amplifier for use in high-speed resolution pipelined A/D converters,' IEEE ISCAS 2002, pII-416-9. Square-law Class-AB mosfet output stage opamps offer better performance than Miller compensated types (eg S Rabii 1997, D Ribner 1984) in low power consumption and low voltage applications (better psrr and slew rate). Only 2 stage topology used, with folded cascode first stage and a fully differential output stage(s). This 'cascode compensation' approach provides better performance than simple Miller compensation.
44. **Ramirez-Angulo J**, Carvajal A, et al, 'The Flipped voltage follower: A useful cell for low-voltage low-power circuits,' IEEE ISCAS 2002, pIII-615-8. Technique used to modify bias current of a LTP giving square-law difference linearity and class-AB. 9 recent references.
45. **Ramirez-Angulo J**, Gonzalez-Carvajal R, Torralba A, Nivea C, 'A new class AB differential input stage for implementation of low-voltage high slew rate op-amps and linear transconductors', ICAS 2001 I-671-4. Class-AB input stage and class-AB output stage for high slew rate and low power consumption, both use square-law differencing.
46. **Ramirez-Angulo J**, 'High slew rate, low voltage BiCMOS and bipolar operational amplifier architectures with rail to rail common mode input voltage swing', IEEE ISCAS 1994, p743-6. Composite fet, BiCMOS pairs, square-law differencing class-AB.
47. **Ramirez-Angulo J**, Treece K, 'A second generation linear low voltage BiCMOS OTA', IEEE ICAS 1993, p1172-5. Simulated structures: Multiple outputs, constant bw input stage, Square law differencing & LTP forms. (Repeated from above).

Interesting articles:

48. **Hyogo A**, K. Sekine, 'Low voltage four-quadrant multiplier using square-root circuits based on cmos pair', IEEE ISCAS 1999, pII 274-277. New inherent linearity technique by differencing the square-roots of the outputs of a differential pair (LTP). Useful for low power class-A audio; lower distortion than square-laws (at low levels), and soft companding (very useful in audio).
49. **Eskiyeerli M**, Payne A, Toumazou C, 'State space synthesis of integrators based on the MOSFET square-law', Electron. Lett. 14 March 1996, p505-6. Mosfet structures preferred as most of the latest fab is geared toward the digital mos process. See Aug p1629 for more details. Geometric mean circuit using 4 mosfets are relatively easy, and two of these form an integrator that is tuneable and very linear.
50. **Mahattanakul J**, Toumazou C, 'DC stable CCII-based instantaneous companding integrator,' IEEE ISCAS 1997 p821-4. Current conveyors with minimal degeneration perform Sinh functions at X (low Z) and Z (output) ports simultaneously, and Cosh by mirroring one output side and summing with a constant current pull-up. Tanh is performed by the ubiquitous LTP with mirror load. First order filter is synthesised with a multiplier in the nfb loop, a Tanh to remove the unwanted nonlinear term across Vc, and an expander. This circuit operates with bipolar inputs.
51. **Vlassis S**, Psychalinos C, 'A square-root domain differentiator,' IEEE ISCAS 2002 II-217-220. A First. Uses geometric mean and multiplier (uses square-law differencing). The time-constant is programmable.
52. **Takagi S**, Sato T, Fujii N, 'Area-efficient voltage-feedback type cmos-companding integrator,' IEEE ISCAS 2002 II-205-8. Uses composite cells for OTA (Square-law difference based) and squarer. Triple-well mosfets are more easily available (since 2002) which has previous slowed development of square-law difference technique in ic's.
53. **Berg Y**, Aunet S, Naess O, Hoven M, 'Exploiting Sinh and Tanh shaped Ultra Low-Voltage Floating-Gate Transconductance Amplifiers to reduce harmonic distortion', ICAS 2001, IV-838-841. CMOS inverter or ultra low voltage operation (ULV) with mosfets in deep weak inversion (an exponential V/I), UV activated bias. Vin 0.2Vpk, 5x better, and thd ~0.2% but depends on matching.
54. **Sanchez-Sinencio E**, Silva-Martinez J, 'CMOS transconductance amplifier, architectures and active filters: a tutorial,' IEE Proc. Circuits, Dev. & Syst, Feb 2000, p3-12. Wide range of methods covered. 76 references.

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Supplemental references:

The following references are from 'Variable-Gain, Variable-transconductance, and Multiplication Techniques: A Survey' by Hauser M.W., et al, pp291-322, a chapter in a book edited by Sansen W, et al, 'Analog Circuit Design: MOST RF Circuits, Sigma-Delta Converters, and Translinear Circuits', Kluwer Academic Publishers, 1996.

These references indicate a lot of effort has been put into using mosfets squarelaw relationship to develop novel methods of achieving linear gain for variable gain amplifiers, multipliers and transconductors (OTA's and Current Conveyors) for analog filters. When a very low supply voltage is not required CMOS pairs can be used to overcome the problem of matching nmos and pmos gains - called COMFET's (Composite mosfets) [71, 75, 88, 94, 96, 101, 106]. The differential pair can be modified to provide a linear output square-law difference if the tail current is increased in proportion to the square of the input voltage [65, 67, 74, 78, 80, , 82, 91, 92]. Alternatively, with a constant tail current the drain currents can be linearised before subtraction [93, 102, 107]. These references only cover developments up to about 1993. A more recent edition of this book or similar books should provide more recent developments. (A few recent references can be found above).

Key *[ref] means I have viewed the paper. [Type a] refers to Fig 9a p305 of Hauser's chapter where input voltages are applied independently to the two mosfets gates. [Type b] refers to Fig 9b where the input voltages is applied only to mosfet M3 while mosfets M1 and M2 have their gate voltages series connected. [Type c] refers to Fig 9c which is a 2 mosfet version of type b. [Type d] refers to Fig 9d which is a variant of type a where the input voltages are applied differentially to each mosfet.

[63] O. A. Seriki and R. W. Newcomb. Direct coupled MOS squaring circuit. *IEEE J. of Solid-State Circuits* vol. SC-14 no. 4 pp766-768, August 1979.

[63] D. C. Soo and R. G. Meyer. A four-quadrant NMOS analog multiplier. *IEEE J. of Solid-State Circuits* vol. SC-17 no. 6 pp1174-1178, December 1982.

[64] D. C. Soo and R. G. Meyer. A four-quadrant NMOS analog multiplier. *IEEE J. of Solid-State Circuits* vol. SC-17 no. 6 pp1174-1178, December 1982.

*[65] A. Nedungadi and T. R. Viswanathan. Design of linear CMOS transconductance elements. *IEEE Trans. on Circuits and Systems* vol. CAS-31 no. 10 pp891-894, October 1984.

*[66] Z. Hong and H. Melchior. Analogue four-quadrant CMOS multiplier with resistors. *Electronics Letters* vol. 21 no. 12 pp531-532, June 1985.

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*[68] J. N. Babanezhad and G. C. Temes. A 20-V four-quadrant CMOS analog multiplier. *IEEE J. of Solid-State Circuits* vol. SC-20 no. 6 pp1158-1168, December 1985. [Gilbert type, see Han tutorial IE3 T.CAS-II, Dec 1998, p1550-63]

- *[69] K. Bult and H. Wallinga. A CMOS four-quadrant analog multiplier. *IEEE J. of Solid-State Circuits* vol. SC-21 no. 3 pp430-435, June 1986. [First simple multiplier using mosfets squarelaw, THD 0.14%. Uses mos Gilbert cell. Squarelaw distortion analysis includes effect of channel length modulation and mobility modulation. Different all nmos V/I converter (Cascaded)]
- [70] T. R. Viswanathan. CMOS transconductance element. *Proc. of the IEEE* vol. 74 no. 1 pp222-224, January 1986. [Type d]
- *[71] C. S. Park and R. Schaumann. A high-frequency CMOS linear transconductance element. *IEEE Trans. on Circuits and Systems* vol. CAS-33 no. 11 pp1132-1138, November 1986. [Type d. Uses Comfets]
- [72] S. L. Wong, N. Kalyanasundaram, and C. A. T. Salama. Wide dynamic range four-quadrant CMOS analog multiplier using linearized transconductance stages. *IEEE J. of Solid-State Circuits* vol. SC-21 no. 6 pp1120-1122, December 1986.
- [73] S. L. Garverick and C. G. Sodini. Large-signal linearity of scaled MOS transistors. *IEEE J. of Solid-State Circuits* vol. SC-22 no. 2 pp282-286, April 1987.
- *[74] K. Bult and H. Wallinga. A class of analog CMOS circuits based on the square-law characteristic of a MOS transistor in saturation. *IEEE J. of Solid-State Circuits* vol. SC-22 no. 3 pp357-365, June 1987. [Type b]
- *[75] E. Seevinck and R. F. Wassenaar. A versatile CMOS linear transconductor/square-law function circuit. *IEEE J. of Solid-State Circuits* vol. SC-22 no. 3 pp366-377, June 1987. [Type b. Uses Comfets. "linear" squarelaw class-AB 'is probably a unique capability' to 4Iq with no saturation at higher currents"]
- [76] J. S. Peña-Finol and J. A. Connelly. A MOS four-quadrant analog multiplier using the quarter-square technique. *IEEE J. of Solid-State Circuits* vol. SC-22 no. 6 pp1064-1073, December 1987.
- [77] S. Qin and R. L. Geiger. A ± 5 -V CMOS analog multiplier. *IEEE J. of Solid-State Circuits* vol. SC-22 no. 6 pp1143-1146, December 1987.
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- *[79] B. Nauta and E. Seevinck. Linear CMOS transconductance element for VHP filters. *Electronics Letters* vol. 25 no. 7 pp448-450, March 1989. [Type d]
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